Cumulative Bio-Bibliography
University of California, Merced

Sung-Mo "Steve" Kang
Chancellor
Professor, School of Engineering

July 1, 2008

EMPLOYMENT HISTORY

2007-present Chancellor, University of California, Merced

2007-present Professor Above-Scale of Engineering, University of California, Merced

2001- 2007 Dean, Baskin School of Engineering, UC Santa Cruz, Santa Cruz

2004- 2007 Professor Above-Scale, Electrical Engineering, UC Santa Cruz

2001-2004 Professor Highest Step, Electrical Engineering, UC Santa Cruz

2003-2005 Chaired Visiting Professor, Korean Advanced Institute of Science and Technology (KAIST)

2006 Honored Visiting Professor, Swiss Federal Institute of Technology at Lausanne (EPFL)

1989-2000 Professor, Electrical and Computer Engineering, Univ. of Illinois at Urbana-Champaign

1989-2000 Research Professor, Coordinated Science Laboratory, Univ. of Illinois at Urbana-Champaign

1990-2000 Professor, Computer Science, Univ. of Illinois at Urbana-Champaign

1990-2000 Research Professor, Beckman Institute, Univ. of Illinois at Urbana-Champaign

1993-1996 Founding Director, Center for ASIC Research and Development, University of Illinois at Urbana-Champaign

1995-2000 Head, Department of ECE, Univ. of Illinois at Urbana-Champaign

1985-1989 Associate Professor, Electrical and Computer Engineering, Univ. of Illinois at Urbana-Champaign

1985-1989 Research Associate Professor, Coordinated Science Laboratory

1989 Visiting Professor, Swiss Federal Institute of Technology at Lausanne

1998 Humboldt Visiting Professor, Technical University of Munchen, Germany, Summer 1998

1997 Humboldt Visiting Professor, University of Karlsruhe, Germany

1977-1982 Member of Technical Staff, AT&T Bell Laboratories, Murray Hill, NJ

1982-1985 Supervisor, AT&T Bell Laboratories, Murray Hill, NJ

1977-1984 Visiting Faculty Member, Rutgers University, Piscataway, NJ

1975-1977 Assistant Professor, Rutgers University, Piscataway, NJ

EDUCATION

1975	Ph.D. Electrical Engineering	Univ. of California at Berkeley
1972	M.S. Electrical Engineering	State Univ. of New York at Buffalo
1970	B.S. Electrical Engineering	Fairleigh Dickinson Univ., Teaneck, NJ (Summa Cum Laude)

HONORS AND AWARDS

Myril B. Reed Best Paper Award, 1979

AT&T Bell Laboratories Exceptional Contribution Award, 1984

Best Paper Award, International Conference on Computer Design, 1987

Listed in Incomplete List of Teachers Ranked as Excellent by Students, Univ. of Illinois, 1987, 1993

IEEE Fellow, 1990

AAAS Fellow, 1997

ACM Fellow, 2000

IEEE Computer Society Meritorious Service Award, 1990

IEEE Computer Society Distinguished Service Award, 1990

Associate in the Center for Advanced Study, UIUC, 1991-1992

Founding Editor-in-Chief, IEEE Transactions on VLSI Systems, February 1992 - December 1994

IEEE Darlington Best Journal Paper Award, May 1993

Republic of China National Science Council Distinguished Lecturer, June 1993

SRC Inventor Recognition Award 1993, 1996, 2002

IEEE Circuits and Systems Society Meritorious Service Award, 1994

IEEE Circuits and Systems Society Distinguished Lecturer, 1994-1997

IEEE LEOS Conference Best Student Paper Award (Senior Author), 1995

University of Illinois Charles Marshall Senior University Scholar, 1995

IEEE Graduate Teaching Technical Field Award (worldwide award), 1996

Humboldt Research Award for Senior U.S. Scientists, 1996

Co-Editor, Series in Advances in Design and Analysis of VLSI Systems, Elsevier Science Publishers B. V.

Foreign Member, National Academy of Engineering of Korea, 1997

IEEE CAS Society Technical Achievement Award, 1997

Korea Broadcasting System (KBS) Compatriot Award, 1998

IEEE CAS Golden Jubilee Medal, 1999

SRC Technical Excellence Award, 1999

22nd EOS/ESD Symposium Best Student Paper Award (Senior Author), 2000

IEEE Millennium Medal, 2000

Distinguished Alumnus Award in Electrical Engineering, UC Berkeley, 2001

Low Power Design Contest Award, International Symposium on Low Power Electronics and Design, 2001

IEEE Solid-State Circuits Society Distinguished Lecturer, 2002-2005

IEEE Circuits and Systems Society Distinguished Lecturer, 2003-2005

Chancellor's Stellar Service Award, UC Santa Cruz, 2003

IEEE Mac E. Van Valkenbur Award, IEEE Circuits and Systems Society, 2005

Chang-Lin Tien Education Leadership Award, 2007

Ghandi, King, Ikeda Community Builder Award, Morehouse College, 2007

Distinguished Yonsei Alumnus Award, 2008

ISQED Quality Award, 2008

Distinguished Korean-American Award, 2008

Listed in Who's Who in America, Who's Who in Technology, Who's Who in Engineering, Who's Who in Midwest, Who's Who in Education, American Men and Women in Science

RECENT GOVERNMENT AND PUBLIC SERVICES

Member, Blue Ribbon Task Force on Nanotechnology (BRTFN) (Chair US Rep. Mike Honda) 2005

Member, International Advisory Board for BK21 Program of Korea 2005

President, Silicon Valley Engineering Council 2002-2003

ASEE (American Society for Engineering Education) Public Policy Committee 2003-2005

State of California Leader for ASEE Engineering Deans Capitol Hill visit 2003, 2004, 2005

Member, Executive Advisory Committee, NSF Engineering Research Center for Biomimetic Microelectronic Systems (USC, UCSC, Caltech) 2003-2005

Member, NSF Review Panel for Science, Technology, Engineering, and Mathematics (STEM) Education 2004

International Reviewer, National Science and Engineering Research Council of Canada 2004

Member, Advisory Committee for California Summer Mathematics and Science Education (COSMOS) 2004-2005

Member, Advisory Committee for California Mathematics Engineering Science Achievement (MESA) 2004-2005

GRANT SUPPORT (partial since 1993)

2008-	Memristor and Memristive Systems (pending)	NSF	$ 54,368
2005-2007	Optimization of Self Reverse Biasing For Leakage Reduction	UC/SMART	$ 67,566
2005-2007	Optimization of Self Reverse Biasing For Leakage Reduction	ZMOS Technology, Inc.	$ 99,672
2004-2006	Electronic Properties of Nanowires	NASA	$127,796
2004-2005	MESA School Program	UCOP	$330,000
2004-2005	Low Power High Performance Static-Dynamic Logic	Intel Corp.	$ 40,000
2004-2005	Low Power High Performance Static-Dynamic Logic	UC/Micro	$ 4,376
2003-2004	Analog/Digital Mixed Design	Inha Univ.	$ 40,000
2004-2005	Yonsei University Program	Yonsei Univ.	$465,740
1999-2005	Physical CAD	NSF	$150,000
2002-2004	Low Power Design of Dynamic Circuits	Intel Corp.	$ 80,000
2003-2008	Developing Effective Engineering Pathways	NSF	$2,000,000
2001-2003	Optoelectronic Modeling and Simulation	DARPA	$150,000
2001-2004	Robust and Scalable Low Power High Performance VLSI	SRC	$360,000
2001-2004	Low Power High Performance Static Dynamic Logic	Intel	$120,000
1997-2000	Temperature-Dependent VLSI Delay Analysis	Intel	$120,000

1998-2001	Computer -Aided Design of Reliable Deep Submicron VLSI Circuits	SRC	$180,000
1998-2001	Low-Power High-Performance Circuits for Sub-1V CMOS	SRC	$180,000
1998-2000	ESD Protection for BiCMOS RF Circuits	Motorola	$100,000
1998-2000	Composite CAD for MEMS	DARPA	$110,000
1998-2000	ESD Protection Circuits	LG Semicon	$100,000
1999-2000	SD-Induced On-Chip Termination Resistor Variation And Its Impact on I/O Circuit Performance Degradation	SRC	$ 50,000
1997-1999	I/O Layout Extraction	TI	$ 80,000
1996-1997	Electrothermal Analysis	Intel	$ 40,000
1997-1998	MPEG4 VLSI Engine	ETRI	$100,000
1996-1997	MPEG VLSI	LG	$100,000
1995-1998	VLSI Research	Hwagoksangsa	$150,000
1995-1998	VLSI Interconnect Reliability	TI	$300,000
1994-1995	Modeling and Simulation for VLSI Reliability	SRC	$ 65,000
1986-1996	Design and Analysis of Optoelectronic System Testbed	NSF ERC	$1M+
1994-1997	Reliability CAD System	AF Rome Lab	$180,000
1995-1996	MPEG VLSI	ETRI	$100,000
1996-1997	Modeling, Simulation and Design Guidelines	SRC	$ 65,000
1996-1997	Computer Simulation of Optical Interconnects	DARPA	$ 55,000
1995-1996	Reliability CAD System	AF Rome	$100,000
1995-1996	Electrothermal Simulation of VLSI	Intel Corp.	$ 40,000
1995-1996	Electrothermal Stress Tolerant Deep Submicron Low Power Circuits	JSEP	$ 60,000
1995-1996	Modeling and Simulation for VLSI Reliability	SRC	$ 65,000
1991-1995	High Level Simulation of VLSI	Samsung Electron Co.	$400,000

1994-1995	Computer Simulation of Optical Interconnects	ARPA	$ 65,000
1995-1996	Computer Simulation of Optical Busses	ARPA	$ 50,000
1995-1996	Design Guidelines for EOS/ESD Reliability	TI	$ 30,000
1995-1996	Computer Simulation of Optical Busses	ARPA	$ 65,000
1995-1996	Design Guidelines for EOS/ESD Reliability	TI	$ 30,000
1994-1995	VLSI Layout Automation	Goldstar Electron Co.	$ 50,000
1994-1995	Electrothermal Simulation of VLSI	Intel Corp.	$ 40,000
1994-1995	CAD for Optoelectronics	ETRI	$100,000
1993-1994	Timing Driven VLSI Layout Automation	Goldstar	$ 50,000
1994-1995	Design Guidelines for ESD/EOS Reliability	TI	$ 30,000
1994-1995	ATM Network Research	AT&T	$ 60,000
1993-1994	Computer Simulation of Optical Busses	ARPA	$ 65,000
1993-1994	ESD/EOS Reliability Analysis	Intel	$ 50,000
1993-1994	ESD/EOS Simulation	ESD/EOS Society	$ 10,000
1993-1994	Design Guidelines for EOS/ESD Reliability	Texas Instruments	$ 40,000
1993-1994	VLSI Layout Synthesis	Motorola	$ 45,000
1993-1994	Modeling and Simulation for VLSI Reliability	SRC	$ 67,000
1993-1994	Computer-Aided Design of High-Performance VLSI Circuits	JSEP	$ 40,000
1993-1994	VLSI Reliability	AMD	$ 50,000

PATENTS

1. U.S. Patent 4,396,994, Data shifting and rotating apparatus, August 2, 1983

2. U.S. Patent 5,404,041, Source contact placement for efficient ESD/EOS protection in grounded-substrate MOS ICs, April 4, 1995

3. U.S. Patent 5,450,267, New ESD/EOS protection circuits for integrated circuits fabricated in advanced n-well CMOS processes, September 12, 1995

4. U.S. Patent 5,610,774, Optical communications and interconnection networks having optoelectronic switches and direct optical routers, March 11, 1997

5. U.S. Patent 5,796,638, Methods, apparatus and computer program products for synthesizing integrated circuits with electrostatic discharge capability and correcting ground rules faults therein, August 18, 1998

6. U.S. Patent, 5,923,656, Scalable broadband input-queued ATM switch including weight driven cell scheduler, July 13, 1999

7. US Patent 6,624,665B2, CMOS Skewed Static Logic and Method of Synthesis, Sept. 23, 2003

8. US Patent 6,759,873, Reverse Biasing Logic Circuit, July 6, 2004

9. US Patent 6,784,694B, CMOS Sequential Logic Configuration for a Double-Edge Triggered Flip-Flop, August 31, 2004

10. US Patent 6,784,707, Delay Locked Loop Clock Generator, August 31, 2004

11. US Patent 6,794,903, CMOS Parallel Dynamic Logic and Speed Enhanced Static Logic, Sept. 21, 2004

12. US Patent 6,900,690, Low Power High Performance Integrated Circuit Architectures and Related Methods

13. US Patent 6,946,901, Low-Power High-Performance Integrated Circuits and Related Methods, Sept. 20, 2005

14. US Patent 6,977,528, Event Driven Dynamic Logic for Reducing Power Consumption, Dec. 20, 2005

15. US Patent 6,861,911, Self-Regulating Voltage-Controlled Oscillator, March 1, 2005

PUBLICATIONS

Books

1. Y. Leblebici and S. M. Kang, Hot-Carrier Reliability of MOS VLSI Circuits, Kluwer Academic Publishers, 1993.

2. S. Sapatnekar and S. M. Kang, Design Automation for Timing-Driven Layout Synthesis, Kluwer Academic Publishers, 1993.

3. M. Sriram and S. M. Kang, Physical Design for Multichip Modules, Kluwer Academic Publishers, 1994.

4. C. H. Diaz, S. M. Kang and C. Duvvury, Modeling of Electrical Overstress in Integrated Circuits, Kluwer Academic Publishers, 1994.

5. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 1995. (Chinese Translation)

6. J. J. Morikuni and S. M. Kang, Computer-Aided Design of Optoelectronic Integrated Circuits and Systems, Prentice Hall, 1996.

7. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, Taiwan, Second Edition, 1998. (Chinese Translation by Hwang Jung-kwang et al.)

8. Y. K. Cheng, C. H. Tsai, C. C. Teng, and S. M. Kang, Electrothermal Analysis of VLSI Systems, Kluwer Academic Publishers, 2000.

9. S. M. Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, Third Edition, 2003

10. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Publishing House of Electronics Industry, Beijing (Chinese Translation by Wang Zi-Gong, et al.)

Books Edited or Co-Edited

Co-Editor, Series in Advances in Design and Analysis of VLSI Systems, Elsevier Science Publishers B. V.
Chapter Editor, Computer-Aided Design and Optimization, The Circuits and Filters Handbook, CRC Press, 1995

Chapter Editor, VLSI and ASIC, VLSI Handbook, CRC Press, 1999

Section Editor, The Circuits and Filters Handbook, Section VII, Computer-Aided Design and Optimization, CRC Press, 2003, pp. 1245-1356

Chapters in Books

1. S. M. Kang and H. Y. Chen, "Circuit Optimization for CMOS VLSI," book chapter, *Advances in Computer-Aided Engineering Design*, JAI Press, Inc., pp. 107-157, 1990.

2. P. Gee, M. Y. Wu, I. N. Hajj, S. M. Kang and W. Shu, "Automatic Circuit Synthesis Using Switching Network Logic and Metal-metal Matrix Layout," JAI Press, Inc., pp. 57-106, 1990.

3. S. M. Kang and M. Sriram, "Binary Techniques for Placement and Routing," book chapter, Algorithmic Aspects of VLSI Layout, World Scientific, pp. 25-68, 1994.

4. S. M. Kang and A. Dharchoudhury, “Modeling of Circuit Performances,” book chapter, pp. 1375-1391, The Circuits and Filters Handbook, CRC Press, 1995.

5. C. W. Kim and S. M. Kang, “Low Power Flip-Flop and Clock Network Design Methodologies in High-Performance System-on-Chips (SOCs), Chapter 7, pp. 151-179, *Power Aware Design Methodologies* (M. Pedram, editor), 2002.

6. K. W. Kim, K. H. Baek, and S. M. Kang, “Coupling-Driven Signal Encoding Schemes for Low Power Interface Design, in *Signal Integrity Effects in Custom IC and ASIC Designs*, Ramionderpal Singh (editor), IEEE Press, Piscataway, NJ and Wiley-Interscience, New York, NY, 2002.

Refereed Journals

1. P. Scott and S. M. Kang, "Stability Properties of a Purkinje Fiber Model," *Computers in Biology and Medicine*, vol. 4, pp. 19-25, June 1974.

2. L. O. Chua and S. M. Kang, "Memristive Devices and Systems," *Proceedings of the IEEE*, Vol. 64, No. 2, pp. 209-223, February 1976.

3. S. M. Kang, "Comments on a Method of Obtaining System Functions Using Δ-M," *Proceedings of the IEEE*, Vol. 65, No. 3, pp. 494, March 1977.

4. L. O. Chua and S. M. Kang, "Sectionwise Piecewise-Linear Functions: Canonical Representation Properties and Applications," *Proceedings of the IEEE (Special Issue on Multidimensional Systems)*, Vol. 65, No. 6, pp. 915-929, June 1977.

5. S. M. Kang and L. O. Chua, "A Global Representation of Multidimensional Piecewise-Linear Functions," *IEEE Transactions on Circuits and Systems*, vol. CAS-25, No. 11, pp. 938-940, November 1978.

6. S. M. Kang, Y. Chen, and T. G. Marshall, Jr., "An Optimal Design of Split-Electrode CCD Transversal Filters," *IEEE Transactions on Circuits and Systems*, Vol. CAS-27, No. 6, pp. 445-451, June 1980.

7. S. M. Kang, "An Optimal Design of Large-Scale Communication Networks," *IEEE Transactions on Circuits and Systems*, pp. 1169-1175, December 1980.

8. S. M. Kang, "A Design of CMOS Polycells for LSI Circuits," *IEEE Transactions on Circuits and Systems*, Vol. CAS-28, No. 8, pp. 838-843, August 1981.

9. S. M. Kang, R. H. Krambeck, H. F. Law, and A. D. Lopez, "Gate Matrix Layout of Random Control Logic in a 32-bit CMOS CPU Chip Adaptable to Evolving Logic Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-2, No. 1, pp. 18-29, January 1983.

10. S. M. Kang, "Simulation of Power Dissipation in VLSI Circuits," *IEEE Journal of Solid-State Circuits*, vol. SC-21, no. 5, pp. 889-891, October 1986.

11. S. M. Kang, "Domino CMOS Barrel Switch for 32-Bit VLSI Processors," *IEEE Circuits and Devices*, vol. 3, no. 3, pp. 3-8, May 1987.

12. S. M. Kang, "Physical Design of Microprocessors," *IEEE Design and Test of Computers*, vol. 4, no. 3, pp. 10-11, June 1987.

13. S. M. Kang, "Metal-Metal Matrix-N^3 for High-Speed VLSI Layout," *IEEE Transaction on Computer-Aided Design,* vol. CAD-6, no. 5, pp. 886-891, September 1987.

14. T. K. Yu, S. M. Kang, I. N. Hajj and T. N. Trick, "Statistical Performance Modeling and Parametric Yield Estimation of MOS VLSI," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. CAD-6, no. 6, pp. 1013-1022, November 1987.

15. D. K. Hwang, W. K. Fuchs and S. M. Kang, "An Efficient Approach to Gate Matrix Layout," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. CAD-6, no. 5, pp. 802-809, December 1987.

16. M. E. Mokari-Bolhassan and S. M. Kang, "Analysis and Correction of VLSI Delay Measurement Errors due to Transmission Line Effects," *IEEE Trans. on Circuits and Systems*, vol. CAS-35, no. 1, pp. 19-25, January 1988.

17. W. Shu, M. Y. Wu, and S. M. Kang, "Improved Net Merging Method for Gate Matrix Layout," *IEEE Transactions on Computer-Aided Design*, vol. CAD-7, no. 9, pp. 947-951, September 1988.

18. W. J. Welch, T. K. Yu, S. M. Kang, and J. Sacks, "Computer Experiments for Quality Control by Parameter Design," *Journal of Quality Technology*, vol. 22, no. 1, pp. 15-22, January 1990.

19. S. M. Kang and H. Y. Chen, "A Global Delay Model for Domino CMOS Circuits," *International Journal on Circuit Theory and Applications*, vol. 18, no. 3, pp. 289-306, May 1990.

20. D. S. Gao, A. T. Yang, and S. M. Kang, "Accurate Modeling and Simulation of Interconnection Delays and Crosstalks in High-Speed Integrated Circuits," *IEEE Transaction on Circuit and Systems*, vol. 37, no. 1, pp. 1-9, January 1990.

21. P. Gee, M. Y. Wu, S. M. Kang, and I. N. Hajj, "A Metal-Metal Cell Generator for Multi-Level Metal MOS Technology, *Integration, the VLSI Journal*, vol. 9, no. 1, pp. 25-47, February 1990.

22. D. S. Gao, S. M. Kang, R. P. Bryan, and J. J. Coleman, "Modeling of Quantum Well Laser for Computer-Aided Analysis of Optoelectronic Integrated Circuits," *IEEE Transaction on Quantum Electronics*, vol. 37, no. 7, pp. 1206-1216, July 1990.

23. P. Gee, M. Y. Wu, S. M. Kang, and I. N. Hajj, "Automatic Synthesis of Metal-Metal Matrix Layout," *Int. J. of Comput.-Aided VLSI Des.*, Vol. 2, no. 1, pp. 83-104, 1990.

24. C. H. Diaz, S. M. Kang and Y. Leblebici, "An Accurate Analytical Delay Model for BiCMOS Driver Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 10, no. 5, P. Gee, M. Y. Wu, I. N. Hajj, S. M. Kang and W. Shu, "Automatic Circuit Synthesis Using Switching Network Logic and Metal-metal Matrix Layout," JAI Press, Inc., pp. 57-106, 1990.

25 A. T. Yang, S. M. Kang, and G. C. Yang, "An Integrated System for Device Model Design, Circuit Simulation, and Parameter Extraction," Advances in Electrical Engineering, *Electrosoft Journal*, (ed. P. P. Silvester), pp. 31-43, Computational Mechanics Publications Springer-Verlag, 1990.

26. D. Zhou, F. P. Preparata, and S. M. Kang, "Interconnection Delay in Very High- Speed VLSI," *IEEE Trans. on Circuits and Systems*, vol. 38, no. 7, pp. 779-790, July 1991. (**IEEE Darlington Paper Award**)

27. P. Duchene, M. Declercq, and S. M. Kang, "A Simple CMOS Transition Accelerator Circuit," *Electronics Letters,* pp. 300-301, February 1991.

28 H. Y. Chen and S. M. Kang, "iCOACH: A Circuit Optimization Aid for CMOS High-Performance Circuits," *Integration, the VLSI Journal*, vol. 10, no. 2, pp. 185-212, January 1991.

29. H. Y. Chen and S. M. Kang, "A New Circuit Optimization Technique for High Performance CMOS Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 10, no. 5, pp. 670-677, May 1991.

30. T. K. Yu, S. M. Kang, W. Welch, and J. Sacks, "Parametric Yield Optimization of CMOS Analog Circuits by Quadratic Statistical of Circuit Performance Models," *International Journal of Circuit Theory and Applications*, vol. 19, pp. 579-592, November 1991.

31. G. M. Tharakan and S. M. Kang, "A New Design of a Fast N-Bit Barrel Switch Network," *IEEE Journal of Solid-State Circuits*, Vol. 27, no. 2, pp. 217-221, February 1992.

32. Y. Leblebici and S. M. Kang, "Modeling of nMOS Transistors for Simulation of Hot-Carrier Induced Device and Circuit Degradation," *IEEE Trans. on Computer-Aided Design*, vol. 11, no. 2, pp. 235-246, February 1992.

33. A. Ketterson, M. Tong, J.-W. Seo, K. Nummila, J. Morikuni, K. Y. Cheng, I. Adesida, and S. M. Kang, "A Submicron Pseudomorphic MODFET-based OEIC Receiver," *IEEE Photonics Technology Letters*, vol. 4, no. 1, pp. 73-76, January 1992.

34. A. Ketterson, M. Tong, J. W. Tong, K. Nummila, J. Morikuni, S. M. Kang, and I. Adesida, "A high-performance AlGaAs/InGaAs/GaAs pseudomorphic MODFET-based monolithic optoelectronic receiver," *IEEE Photonics Tech. Lett4,* p. 73, 1992.

35. A. Ketterson, M. Tong, J. W. Tong, K. Nummila, K. Y. Cheng, J. Morikuni, S. M. Kang and I. Adesida, "Submicron modulation-doped field-effect-transistor/metal-semiconductor-based optoelectronic integrated circuit receiver fabricated by direct-write electron beam lithography," *J. of Vac. Sci. and Tech. B10*, p. 2936, 1992.

36. J. J. Morikuni, D. S. Gao, and S. M. Kang, "Modeling of Optical Logic Gates for Computer Simulation," *IEE Proceedings-J, Optolectronics,* vol. 139, no. 2, pp. 105-116, April 1992.

37. Y. H. Shih and S. M. Kang, "Analytic Transient Solution of General MOS Circuit Primitives," *IEEE Transactions on Computer-Aided Design,* vol. 11, no. 6, pp. 719-731, June 1992.

38. C. H. Diaz and S. M. Kang, "New Algorithms for Circuit Simulation of Device Breakdown," *IEEE Trans. on Computer-Aided Design*, vol. 11, no. 11, pp. 1344-1354, November 1992.

39. R. Thaik, N. Lek, and S. M. Kang, "A New Global Router using Zero-One Linear Integer Programming Techniques for Sea-of-Gates and Custom Logic Arrays," *IEEE Transactions on Computer-Aided Design*, vol. 11, no. 12, pp. 1479-1494, December 1992.

40. J. J. Morikuni and S. M. Kang, "An Analysis of Inductive Peaking in Photoreceiver Design," *IEEE Journal of Lightwave Technology*, vol. 10, no. 10, pp. 1426-1437, October 1992.

41. E. C. Chang and S. M. Kang, "Computationally Efficient Simulation of Lossy Transmission Line by Using Numerical Inverse Laplace Transform," *IEEE Trans. on Circuits and Systems*, (Spec. issue on Simulation, Modeling, and Electrical Design of High-Speed and High-Density Interconnects), vol. 39, no. 22, pp. 861-868, November 1992.

42. M. S. Unlu, Y. Leblebici, S. M. Kang, and H. Morkoc, "Transient Simulation of Resonant Cavity Enhanced heterojunction Photodiodes Under Pulse Illumination," *IEEE Photonics Technology Letters,* vol. 4, no. 12, pp. 1366-1369, December 1992.

43. S. G. Bishop, I. Adesida, J. J. Coleman, T. A. DeTemple, M. Feng, K. Hess, N. Holonyak, Jr., S. M. Kang, G. E. Stillman, and J. T. Verdeyen, "The Engineering Research Center for Compound Semiconductor Microelectronics," *Proc. of the IEEE,* vol. 81, no. 1, pp. 132-151, January 1993.

44. Y. Leblebici, W. Sun, and S. M. Kang, "Parametric Macromodeling of Hot-Carrier Induced Dynamic Degradation in MOS VLSI Circuits," *IEEE Transactions on Electron Devices,* vol. , no. 40, no. 3, pp. 673-676, March 1993.

45. Y. Leblebici and S. M. Kang, "Modeling and Simulation of Hot-Carrier Induced Device Degradation in MOS Circuits," *IEEE Journal of Solid-States Circuits*. vol. 28, no. 5, pp. 585-595, May 1993.

46. Y. H. Shih, Y. Leblebici, and S. M. Kang, "ILLIADS: A Fast Timing and Reliability Simulator for Digital MOS Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 12, no. 9, pp. 1387-1402, November 1993.

47. A. A. Ketterson, J. -W. Seo, M. Tong, K. Nummila, J. J. Morikuni, K.-Y. Cheng, S. M. Kang, and I. Adesida, "A MODFET-Based Optoelectronic Integrated Circuit Receiver for Optical Interconnects," *IEEE Trans. on Electron Devices,* vol. 40, no.8, pp. 1406-1446, August 1993.

48. S. Sapatnekar, V. B. Rao, P. M. Vaidya, and S. M. Kang, "An Transistor Sizing Problem for CMOS Circuits Using Convex Optimization," *IEEE Trans. on Computer-Aided Design,* vol. 12, no. 11, pp. 1621-1634, November 1993.

49. C. H. Diaz, C. Duvvury, S. M. Kang, and L. Wagner, "Electrical Overstress Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices," *Journal of Electrostatics*, vol. 31, pp. 161-176, November 1993.

50. C. H. Diaz, S. M. Kang, and C. Duvvury, "Electrical Overstress Thermal Failure Simulation for Integrated Circuits," *IEEE Transactions on Electron Devices*, vol. 41, no. 3, pp. 359-366, March 1994.

51. C. H. Diaz and S. M. Kang, "Circuit-Level Electro-Thermal Simulation of Electrical Overstress Failures in Advanced MOS I/O Protection Devices," *IEEE Trans. on Computer-Aided Design*, vol. 13, no. 4, pp. 482-493, April 1994.

52. Y. Leblebici and S. M. Kang, "Simulation of Hot Carrier Induced MOS Circuit Degradation for VLSI Reliability Analysis," *IEEE Transactions on Reliability*, vol. 43, no. 2, pp. 197-206, June 1994.

53. J. J. Morikuni, A. Dharchoudhury, Y. Leblebici, and S. M. Kang, “Improvements to the Standard Theory of Photoreceiver Noise, *IEEE J. Of Lightwave Technology,* vol. 12, no. 7, pp. 1174-1184, July 1994.

54. S. S. Sapatnekar, P. M. Vaidya, and S. M. Kang, “Convexity-Based Algorithms for Design Centering,” *IEEE Transactions on Computer-Aided Design,* vol. 13, no. 12, pp. 1536-1549, December 1994.

55 C. H. Diaz, C. Duvvury, and S. M. Kang,”Studies of EOS Susceptibility in 0.6um nMOS ESD I/O Protection Structures,” Journal of Electrostatics, 33, pp. 273-289, 1994.

56 R. M. Lammert, P. V. Mena, D. V. Forbes, M. L. Osowski, S. M. Kang, and J. J. Coleman, "Strained-Layer in GaAs-AlGaAs Lasers with Monolithically Integrated Photodiodes by Selective-Area MOCVD," *IEEE Photonics Tech. Lett.*, Vol. 7, no. 3, pp. 247-250, March 1995.

57. D. H. Cho, S. M. Kang, K.-H. Kim, and S.-H. Lee, "An Accurate Intrinsic Capacitance Modeling for Deep Submicron MOSFETs," *IEEE Trans. on Electron Devices*, Vol. 42, no. 3, pp. 540-548, March 1995.

58. A. Dharchoudhury and S. M. Kang, "Worst-Case Analysis and Optimization of VLSI Circuit Performances," *IEEE Trans. on Comput.-Aided Des.*, Vol. 14, no. 4, pp. 481-492, April 1995.

59. B. K. Whitlock, J. J. Morikuni, E. Conforti, and S. M. Kang, "Simulating Optical Interconnects," *IEEE Circuit and Devices*, Vol. 11, no. 3, pp. 12-18, May 1995.

60. J. Lockwood, H. Duan, J. J. Morikuni, S. M. Kang, S. Akkineni, and R. H. Campbell, "Scalable Optoelectronic ATM Networks: The iPOINT Fully Functional Testbed," *IEEE J. of Lightwave Technol.*, Vol. 13, no. 6, pp. 1093-1103, June 1995.

61. J. H. Kim, D. Y. Han, M. H. Nam, and S. M. Kang, "Analysis of Three-Layered Piezoelectric Ceramic Transformer Filter," *IEEE Trans. on Circuits and Syst., Part I*, Vol. 42, no. 6, pp. 307-313, June 1995.

62. M. Sriram and S. M. Kang, "Efficient Approximation of the Time-Domain Response of Lossy Coupled Transmission Line Trees," *IEEE Trans. on Comput.-Aided Des. of Integrated Circuits and Syst.*., Vol. 14, no. 8, pp. 1013-1024, August 1995.

63. S. A. Javro and S. M. Kang, "Transforming Tucker's Linearized Laser Rate Equations to a Form that has a Single Solution Regime," *IEEE J. Lightwave Tech.*, Vol. 13, no. 9, pp. 1899-1904, September 1995.

64. E. Brauer and S. M. Kang, "An Algorithm for Functional Verification of Digital ECL Circuits," *IEEE Trans. on Comput.-Aided Des.*, Vol. 14, no. 12, 1546-1556, December 1995.

65. J. Kim and S. M. Kang, "A New Triple-Layer OTC Channel Router," *IEEE Trans. on Comput.-Aided Des.*, vol. 15, no. 9, pp. 1059-1070, September 1996.

66. E. Chang and S. M. Kang, "Transient Simulation of Lossy Coupled Transmission Lines using Interative Linear Least Square Fitting and Piecewise Recursive Convolution," *IEEE Trans. on Circuits and Syst., Part I.*, vol. 43, no. 11, pp. 923-932, November 1996.

67. A. Xiang, W. Wohlmuth, P. Fay, S. M. Kang and I. Adesida, "Modelling of InGaAs MSM Photodetector for Circuit-Level Simulation," *IEEE J. of Lightwave Technol.*, vol. 14, no. 5, pp. 716-723, May 1996.

68. P. Mena, S. M. Kang, and T. A. DeTemple, "Rate-Equation-Based Laser Models with a Single Solution Regime," *IEEE J. of Lightwave Tech.,* vol. 15, no. 4, pp. 717-730, April 1997.

69. B. K. Whitlock, P. K. Pepeljugoski, D. M. Kuchta, J. D. Crow, and S. M. Kang, "Computer Modeling and Simulation of the Optoelectronic Technology consortium (OETC) Optical Bus," *IEEE J. on Selected Areas in Communications*, vol. 15, no. 4, pp. 6-18, May 1997.

70. C.-C. Teng, Y.-K. Cheng, E. Rosenbaum, and S. M. Kang, "iTEM: A Temperature-Dependent Electromigration Reliability Diagnosis Tool," *IEEE Trans. on Comput.-Aided Des. of Integrated Circuits and Syst.,* vol. 16, no. 8, pp. 882-894, August 1997.

71. H. Kutuk and S. M. Kang, "Filer Design Using a New Field Programmable Analog Array," *Analog Integrated Circuits and Signal Processing,* vol. 14, no.1/2, pp. 81-90, September 1997.

72. L. P. Yuan, C. C. Teng, and S. M. Kang, "Statistical Estimation of Average Power Dissipation using Nonparametric Techniques," *IEEE Trans. on VLSI Syst.*, Vol. 6, no. 1, pp. 65-73, March 1998.

73. J. W. Stroming, Y. Kang, S. M. Kang, and T. S. Huang, "New Architectures for M4R Shape Coding," *IEEE Trans. Circuits Syst.*, Part II, Vol. 45, no. 5, pp. 556-562, May 1998.

74. Y. Huh, Y. Sung, and S. M. Kang, "A Study of Hot-Carrier-Induced Mismatch Drift: A Reliability Issue for VLSI Circuits," *IEEE J. of Solid-State Circuits*, Vol. 33, no. 6, pp. 921-927, June 1998.

75. Y.-K. Cheng, P. Raha, C.-C. Teng, E. Rosenbaum, and S. M. Kang, "ILLIADS-T: An Electrothermal Timing Simulator for Temperature-Sensitive Reliability Diagnosis of CMOS VLSI Chips," IEEE Trans. on Comput.-Aided Des., Vol. 17, no 8, pp. 668-681, August 1998.

76. L. P. Yuan and S. M. Kang, "Average Power Analysis of Sequential Circuits Using an Autoregressive Model," *Circuits, Systems and Signal Processing,* Birkhäusêr, vol. 17, no. 2, pp. 289-304, 1998.

77. H. Kutuk and S. M. Kang, "A Switched Capacitor Approach to Field-Programmable Analog Array Design," *Analog Integrated Circuits and Signal Processing,* vol. 17, pp. 51-65, 1998.

78. J. J. Morikuni, P. V. Mena, A. V. Harton, K. W. Wyatt, and S. M. Kang, "Spatially Independent VCSEL Models for the Simulation of Diffusive Turn-Off Transients," *J. of Lightwave Technology,* vol. 17, no. 1, pp. 95-102, January 1999.

79. H. Kutuk, I. C. Goknar, and S. M. Kang, "Interconnect Simulation in a Fast Timing Simulator ILLIADS-I," *IEEE Trans on Circuits and Syst.-1,* vol. 46, no. 1, pp. 178-189, January 1999.

80. S. M. Yoo and S. M. Kang, " Improved Domino Structures Effective for High Performance Design," *Electronic Letters*., Vol. 35, no. 5, pp. 367-368, March 1999.

81. E.Conforti, A. C. Bordonalli, S. Ho, and S. M. Kang, "Optical 2R Demodulator using Feed-Forward Control of Semiconductor Optical Amplifier Gain," *Microwave and Optical Technol. Lett*., Vol. 21, no. 1, pp. 39-42, April 5, 1999.

82. P. V. Mena, J. J. Morikuni, S. M. Kang, A. V. Harton, and K. W. Wyatt," A Simple Rate-Equation-Based Thermal VCSEL Model," *IEEE J. of Lightwave Technol*., Vol. 17, no. 5, pp. 865-872, May 1999.

83. A. Hossain, S.-M. Kang, and R. Horst, "ServerNet and ATM Interconnects: Comparison for Compressed Video Transmission," *J. of Commun*., Vol. 1, no. 2, pp. 134-142, June 1999.

84. P. V. Mena, J. J. Morikuni, S. M. Kang, A. V. Harton, and K. W. Wyatt, "A comprehensive circuit-level model of vertical-cavity surface-emitting lasers," *IEEE J. of Lightwave Technol*., Vol. 17, no. 2, pp. 2612-2632, December 1999.

85. D. Chen, E. Rosenbaum, and S. M. Kang, "Interconnect Thermal Modeling for Accurate Simulation of Circuit Timing and Reliability," *IEEE Trans. on Comput.-Aided Des*., Vol. 19, no. 2, February 2000.

86. C. H. Tsai and S. M. Kang, "Cell-Level Placement for Improving Substrate Thermal Distribution," *IEEE Trans. on Comput.-Aided Des.*, Vol. 19, no. 2, February 2000.

87. S. O. Jung and S. M. Kang, "Modular Charge Recycling Pass Transistor Logic (MCRPL)," *IEE Electronic Lett,*vol. 36, no. 5, pp. 404-405, March 2000.

88. C. Kim, S. M. Yoo, and S. M. Kang, "Low Power Adiabetic Computing with NMOS Energy Recovery Logic," *IEE Electronics Letters,* vol. 36, no. 16, pp. 1349-1350, August 2000.

89. Y. K. Cheng and S. M. Kang, "A Temperature-Aware Simulation Environment for Reliable ULSI Chip Design," *IEEE Trans. On Comput.-Aided Des.,* vol. 19, no. 10, pp. 1211-1220, Oct. 2000.

90. I. C. Goknar, H. Kutuk, and S. M. Kang, "MOMCO: Method of Moment Components for Passive Model Reduction of RLCG Interconnects," *IEEE Trans. On Circuits and Syst.,Part I,* vol. 48, no. 4, pp. 459-474, April 2001.

91. I. C. Hwang and S. M. Kang, "Differential Pass Transistor Clocked Flip-Flop," *Electronics Letters,* vol. 37, no. 12, pp. 732-734, June 2001.

92. K. W. Kim and S. M. Kang, "Crosstalk Noise Minimization in Domino Logic Design," *IEEE Trans. on Computer-Aided Des.,* vol. 20, no. 9, pp. 1091-1100, Sept. 2001.

93. K. W. Kim, C. L. Liu and S. M. Kang, "Domino Logic Synthesis Based on Implication Graph," *IEEE Trans. on Computer-Aided Desig,* vol. 21, No.2, pp. 232-240, February 2002.

94. C. W. Kim, S. O. Jung, K. H. Baek and S. M. Kang, "High-Speed CMOS Circuits with Parallel Dynamic Logic and Speed-Enhanced Skewed Logic," *IEEE Trans. On Circuits and System,* vol. 49, no. 6, pp. 434-439, June 2002.

95. K. W. Kim, T. W. Kim, T. T. Hwang, C. L. Liu and S. M. Kang, "Logic Transformation for Low Power Synthesis," ACM Trans. On Design Automation of Electronic Systems (TODAES), vol. 7, no. 2, pp. 1-19, April 2002.

96. C. W. Kim and S. M. Kang, "A Low-Swing Clock Double-Edge Triggered Flip-Flop," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 7, pp. 648-652, May 2002

97. S. O. Jung, K. W. Kim, and S. M. Kang, "Noise Constrained Power Optimization for Dual Vt Domino Logic," *IEEE Trans. On VLSI,* Vol. 10, no. 5, pp. 532-541, Oct. 2002.

98. S.O. Jung, S.M. Kang, "High Performance Dynamic Logic Incorporating Gate Voltage Controlled Keeper Structure for Wide Fan-In Gate," IEEE Electronics Letters, Vol 38, No. 16, Pages 852-853, 1 Aug. 2002.

99. C. W. Kim and S. M. Kang, "A Low-Power Small-Area +/- 7.28pS Jitter 1GHz DLL-Based Clock Generator, *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1414-1420, November 2002.

100. S. O. Jung, K. W. Kim, and S. M. Kang, "Time Constraints for Domino Logic Gates with Time-Dependent Keepers," *IEEE Trans. On CAD*, vol. 22, no. 1, pp. 96-103, Jan. 2003.

101. J. S. Lee, K. W. Kim, Y. J. Huh, P. Bendix, and S. M. Kang, "Chip-Level Charged-Device Modeling and Simulation in CMOS Integrated Circuits," *IEEE Trans. On CAD*, vol. 22, no. 1, pp. 67-81, Jan. 2003.

102. C. W. Kim, K. W. Kim, and S. M. Kang, "Energy Efficient Skewed Static Logic Design with Dual Vt," *IEEE Trans. On VLSI,* vol. 11, no. 1, pp. 64-70, Feb. 2003.

103. K. W. Kim, S. O. Jung, U. Narayana, C. L. Liu, and S. M. Kang, "Noise-Aware Interconnect Power Optimization in Domino Logic Synthesis," *IEEE Trans. On VLSI*, vol. 11, no. 1, pp. 79-89, Feb. 2003.

104. K.W. Kim, S.O. Jung, T. Kim, S.M. Kang, "Minimum Delay Optimization for Domino Circuits — a Coupling-Aware Approach." *ACM Trans. Design Autom. Electr. Syst.* 8(20), pp. 202-213, 2003.

105. J. H. Chen, J. Zou, C. Liu, J. E. Schutt-Aine, and S. M. Kang, "Design and Modeling of Micromachined High-Q Capacitor With Large Tuning Range and a Vertical Planar Spiral Inductor," *IEEE Trans. On Electron Devices,* vol. 50, no. 3, pp. 730-739, March 2003.

106. K. W. Kim, S. O. Jung, P. Saxena, C. L. Liu, and S. M. Kang, "Coupling Delay Optimization by Temporal Decorrelation Using Dual Threshold Voltage Technique," *IEEE Trans. On VLSI*, vol. 11, no. 5, pp. 272-276, March 2007.

107. J. H. Chen, J. Zou, C. Liu, and S. M. Kang, "Reduced-Order Modeling of Weakly Nonlinear MEMS Devices with Taylor Series Expansion and Arnoldi Approach," *IEEE J. of Electromechnical System,* vol. 13, no. 3, pp. 441-451, June 2004.

108. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Design of ESD Power Protections with Diode Structures for Mixed-Signal Power Systems," *IEEE J. of Solid-State Circuits,* vol. 39, no. 1, pp. 260-264, Jan. 2004.

109. I. C. Hwang, C. W. Kim, and S. M. Kang, "A CMOS Self Regulating VCO with Low Supply Sensitivity, *IEEE J. of Solid-State Circuits* vol. 39, no. 1, pp. 42-48, Jan. 2004.

110. Ge Yang and S. M. Kang, "A 32-bit Carry Lookahead Adder Using Dual-Path All-N Logic," *IEEE Trans.On VLSI*, Vol. 13, no. 8, pp. 992-996, Aug. 2005

111. J. L. Tsai, C. P. Chen, G. Goplen, H. Qian, Y. Zhan, S. M. Kang, D. F. Wong, S. Sapatnekar, "Temperature-Aware Placement of SOCs," *Proc. of the IEEE, Sepcial Issue on On-Chip Thermal Engineering*, pp. 1502-1518, August 2006

112. S. H. Shin, K. Kim, K. Lee, and S. M. Kang, "Fast Frequency Offset Cancellation Loop using Low-IF Receiver and Fractional-N PLL," *IEEE Trans. On Circuits and Systems II*, vol. 54, no. 3, pp. 272-276, March 2007.

113. G. Yang, Z. Wang and S. M. Kang, "Gate Leakage Tolerant Circuits in Deep Sub-100nm CMOS Technologies," *Special Issue on Microelectronics MEMS and Nanotechology of Smart Materials and Structures,* 15 S21-S28, February 2006.

114. J. Hu, Y. Liu, C.Z. Ning, R. Dutton, and S.M. Kang, "Fringing Field Effects on Electrical Resistivity of Semiconductor Nanowire-Metal Contacts," *Appl. Phys. Lett.* 92, 083503, 2008.

115. S. Shin, S.M. Kang, "Direct-Digital Transmitter with Reduced Clock Harmonic Effects," *Electronics Letters*, submitted March 2008.

116. S. Shin, K. Kim and S.M. Kang, "Receiver Sensitivity Control Method with Wide-range dB-Linear input programmable Range," *Electronics Letters*, submitted March 2008.

117. S. Shin, K. Lee, and S.M. Kang, "Low-Power Frequency Synthesizer with Fast Settling Time Performance," *IEEE Transactions on Circuits and Systems*, submitted March 2008.

Refereed Conference Proceedings

1. L. O. Chua and S. M. Kang, "A Theory of Memristive Systems, "*Proceedings of Third International Symposium on Network Theory*, Split, Yugoslavia, September 1975.

2. S. M. Kang and L. O. Chua, "A New Analytical Representation for Sectionwise Piecewise-Linear Functions and Its Applications," *Proceedings of the 14th Allerton Conference on Circuit and System Theory*," pp. 667-676, September 1976.

3. S. M. Kang and L. O. Chua, "Modeling of the Steady-State Responses of Nonlinear Devices and Systems," *Proceedings of the International Symposium on Circuits and Systems*, Phoenix, AZ, April 1977.

4. S. M. Kang, Y. Chen, and T. G. Marshall, Jr., "The Optimal Design of CCD Transversal Filters Using Integer Programming Approach," *Proceedings of the International Symposium on Circuits and Systems*, New York, May 1978.

5. S. M. Kang, "An Efficient Design of Large-Scale Communication Networks with a Decomposition Technique," *Proceedings of the 22nd Midwest Symposium on Circuits and Systems*, Philadelphia, PA, June 1979. (**Myril B. Reed Best Paper Award**)

6. S. M. Kang, "Computer-Aided Design of LSI CMOS Polycells," *Proceedings of International Symposium on Circuits and Systems*, April 1980.

7. S. M. Kang, R. H. Krambeck, H. F. Law, and A. D. Lopez, "Gate Matrix Layout of Random Control Logic," *ACM IEEE 19th Design Automation Conference Proceedings*, Las Vegas, NV, pp. 190-194, July 1982.

8. S. M. Kang and H. F. Law, "Automation of VLSI Gate Martix Layout," *Proceedings of International Symposium on Circuits and Systems*, May 1983.

9. S. M. Kang, "Elements of CMOS VLSI System Design," *Proceedings International Workshop on VLSI and CAD*, Seoul, Korea, pp. 1-23, June 1985.

10. S. M. Kang, "Accurate Simulation of Power Dissipation in VLSI Circuits," *Proceedings 19th Asilomar Conference on Circuits, Systems, and Computers*, Pacific Grove, CA, pp. 548-551, November 1985.

11. S. M. Kang, "Circuit Considerations for Ultrasmall Devices, Interconnects and Packaging Structures," (Invited Paper), *Proceedings, Workshop on Technologies of Ultrasmall Electronic Devices*, Clemson, North Carolina, pp. 35-71, May 1986.

12. R. D. Freedman, S. M. Kang, C. G. Lin-Hendel, and M. L. Newby, "Extraction of SPICE Circuit Models from Symbolic Gate Matrix Layout with Pruning," *ACM/IEEE Design Automation Conference Proceedings*, Las Vegas, Nevada, pp. 418-424, June 1986.

13. S. M. Kang and H. Y. Chen, "Modeling of Propagation Delay for a Class of Domino CMOS Circuits," *Proceedings, 29th Midwest Symposium on Circuits and Systems*, Lincoln, Nebraska, pp. 907-910, August 1986.

14. S. M. Kang and D. Chu, "CMOS Circuits Design for Prevention of Single Event Upset," *Proceedings IEEE International Conference on Computer Design,* Port Chester, NY, pp. 385-388, October 1986.

15. S. M. Kang, "The State-of-the-Art in the VLSI CAD," *International Workshop on VLSI CAD*, (Invited Paper), Seoul, Korea, pp. 1-17, October 1986.

16. K. R. Cioffi, A. Yang, T. N. Trick, and S. M. Kang, "A Charge-Conserved Circuit Simulation Model for MODFETs," *Workshop on Numerical Modeling of Processes and Devices of Integrated Circuits*, November 1986.

17. T. K. Yu, S. M. Kang, I. N. Hajj, and T. N. Trick, "Statistical Modeling of VLSI Circuit Performances," *Digest of Technical Papers, IEEE International Conference on Computer-Aided Design*, Santa Clara, California, pp. 224-227, November 1986.

18. D. K. Hwang, W. K. Fuchs, and S. M. Kang, "An Efficient Approach to Gate Matrix Layout," *Digest of Technical Papers, IEEE International Conference on Computer-Aided Design*, Santa Clara, CA, pp. 312-315, November 1986.

19. M. E. Mokari-Bolhassan and S. M. Kang, "VLSI Device Characterization for Accurate Delay Measurements Under Transmission Line Effects," *Proceedings, International Symposium on Circuits and Systems,* pp. 526-529, May 1987.

20. S. M. Kang and J. P. Ebner, "Accurate I/O Timing Measurement of High-Speed VLSI Devices," *Proceedings, 30th Midwest Symposium on Circuits and Systems*, August 1987.

21. J. L. Krysl and S. M. Kang, "The Metastability Properties and Optimization of CMOS Latch Devices," *Proceedings, European Conference on Circuit Theory and Design*, pp. 759-764, September 1987.

22. H. Y. Chen and S. M. Kang, "Performance Optimization for Domino CMOS Circuit Modules," *Proceedings, International Conference on Computer Design,* pp. 522-525, October 1987. (**Best Paper Award**)

23. F. P. Lai, S. M. Kang, T. N. Trick, and V. B. Rao, "iJADE: A Rule-Based Hierarchical CMOS VLSI Circuit Optimizer," *Proceeding, International Conference on Computer Design*, pp. 38-41, October 1987.

24. D. C. Yeh, S. M., Kang and V. B. Rao, "CMOS Logic Circuit Partitioning with Complexity-Based Gate Weighting," *Proceedings, International Conference on Computer Design,* pp. 358-361, October 1987.

25. P. Gee, M. Y. Wu, S. M. Kang, and I. N. Hajj, "Metal-Metal Matrix (M^3) CMOS Cell Generator with Compaction," *Proceedings, International Conference on Computer-Aided Design*, pp. 184-187, November 1987.

26. F. P. Lai, S. M. Kang, and T. N. Trick, "A Timing Error Corrector for VLSI Synchronous Path Circuits," *Proceedings, International Conference on Computer-Aided Design*, pp. 48-51, November 1987.

27. Leblebici, S. M. Kang, C. T. Sah, and T. Nishida, "Modeling and Simulation of Hot Electron Effects for VLSI Reliability," *Proceedings, International Conference on Computer-Aided Design*, pp. 252-255, November 1987.

28. K. Yu and S. M. Kang, "Statistical MOS VLSI Circuit Optimization with Non-Nested Experimental Design," *Proc. 1988 International Symposium on Circuits and Systems,* pp. 1799-1802, June 1988.

29. S. Gao, A. T. Yang, and S. M. Kang, "Accurate Modeling and Simulation of Parallel Interconnects in High-Speed Integrated Circuits," *Proc. 1988 International Symposium on Circuits and Systems,* pp. 2105-2108, June 1988.

30. R. Cioffi, S. M. Kang, and T. N. Trick, "Circuit Simulation Models for the High Electron Mobility Transistor," *Proc. of 1988 International Symposium on Circuits and Systems*, pp. 405-408, June 1988.

31. A. T. Yang, D. S. Gao, and S. M. Kang, "Computer-Aided Simulation of Optical Interconnect for High Speed Digital Systems," *Proc. 1988 International Conference on Computer Design*, pp. 87-90, Oct. 1988.

32. D. Zhou, F. P. Preparata, and S. M. Kang, "Interconnection Delay in Very High-Speed VLSI," *Proc. 1988 International Conference on Computer Design*, pp. 52-55, Oct. 1988.

33. H. Y. Chen and S. M. Kang, "An Efficient Layout Style for Dynamic Functional Cells," *Proc. 1988 Midwest Symposium on Circuits and Systems*, pp. 866-869, August 1988.

34. P. Gee, I. N. Hajj, and S. M. Kang, "iSILVER: A Symbolic Layout Generator for MOS Circuits," *Proc. 1988 Midwest Symposium on Circuits and Systems*, pp. 142-145, August 1988.

35. H. Y. Chen and S. M. Kang, "iCOACH: A Circuit Optimization Aid for CMOS High-Performance Circuits," *Proc. 1988 International Conference on Computer Aided Design*, pp. 372-375, November 1988.

36. S. M. Kang and Y. Leblebici, "An Efficient Method for Circuit Sensitivity Calculation Using Piecewise Linear Waveform Models," *Proc. 1988 International Conference on Computer Aided Design*, pp. 24-27, November 1988.

37. T. K. Yu, S. M. Kang, I. N. Hajj, and T. N. Trick, "iEDISON: An Interactive Statistical Design Tool for MOS VLSI Circuits," *Proc. International Conference on Computer Aided Design*, pp. 20-23, Nov. 1988.

38. A. T. Yang and S. M. Kang, "iSMILE: A Novel Circuit Simulation Program with Emphasis on New Device Model Development," *1989 ACM/IEEE Design Automation Conference*, pp. 630-633, June 1989.

39. Y. H. Shih and S. M. Kang, "Fast MOS Circuit Simulation with a Direct Equation Solver," *Proceedings International Conference on Computer Design*, pp. 276-279, Oct. 1989.

40. H. Y. Chen and S. M. Kang, "Performance Driven Cell Generator for Dynamic CMOS Circuits," *Proceedings International Symposium on Circuits and Systems*, pp. 1883-1886, May 1989.

41. A. T. Yang and S. M. Kang, "iSMILE: A New Device Modeling/Circuit Simulation Program," *1989 International Conference on Circuits and Systems*, pp. 417-420, July 1989.

42. D. S. Gao, A. T. Yang, S. M. Kang, R. P. Bryan, M. E. Givens, and J. J. Coleman, "A Quantum-Well Laser Model for Circuit Simulation," *1989 Topical Meeting on Numerical Simulation and Analysis in Guided-Wave Optics and Optoelectronics*, pp. 15-18, February 1989.

43. Y. Leblebici and S. M. Kang, "Simulation of MOS Parameter Degradation with Emphasis on VLSI Design-For-Reliability," *Proceedings International Conference on Computer Design*, pp. 492-495, Oct. 1989.

44. T. K. Yu, S. M. Kang, W. J. Welch, and J. Sacks, "Parametric Yield Optimization of MOS VLSI Circuits with Statistical Performance Modeling," *Proceedings, 1989 International Conference on Computer-Aided Design*, pp. 190-193, November, 1989.

45. P. Gee, I. N. Hajj, and S. M. Kang, "A Custom Cell Generation System for Double Metal CMOS Technology," *Proceedings, 1989 International Conference on Computer-Aided Design*, pp. 140-143, November, 1989.

46. P. Gee, I. N. Hajj, and S. M. Kang, "An Improved Min-Cut Approach for Gate Matrix and Metal-Metal Matrix Circuit Layout," *32nd Midwest Symposium on Circuits and Systems*, pp. 555-558, Champaign, IL, August 1989.

47. I. N. Hajj, S. M. Kang, and P. Gee, "Automatic Circuit Synthesis for Multilevel Metal MOS Technology," *International Conf. on VLSI and CAD*, Seoul, Korea, pp. 149-153, October 17-20, 1989.

48. S. M. Kang, "Regular Structures for CMOS VLSI Design," *Proceedings International Workshop on CMOS VLSI Design*, (Lausanne, Switzerland, Sept. 1989).

49. S. M. Kang, "Floorplanning for CMOS VLSI Design," *Proceedings International Workshop on CMOS VLSI Design*, (Lausanne, Switzerland, Sept. 1989).

50. Y. Leblebici and S. M. Kang, "A One-Dimensional MOSFET Model for Simulation of Hot-Carrier Induced Device and Circuit Degradation," *Proceedings, International Symposium on Circuits and Systems*, pp. 109-112, May 1990.

51. C. H. Diaz, S. M. Kang, and Y. Leblebici, "An Accurate Analytical Delay Model for BiCMOS Driver Circuits," *Proceedings, International Symposium on Circuits and Systems*, pp. 558-561, May 1990.

52. M. Sriram and S. M. Kang, "A Modified Hopfield Network for Two-Dimensional Module Placement," *Proceedings, International Symposium on Circuits and Systems*, pp. 1164-1169, May 1990.

53. S. M. Kang, "Performance-Driven Layout of CMOS VLSI Circuits," *Proceedings, International Symposium on Circuits and Systems*, pp. 881-884, May 1990.

54. A. T. Yang, S. M. Kang, and G. C. Yang, "An Integrated CAD System for Device Model Design, Parameter Extraction, and Circuit Extraction," *Proceedings of Electrosoft 90*, August 1990.

55. Y. Leblebici and S. M. Kang, "An Integrated Reliability Simulation Tool for Hot Carrier Resistant VLSI Design," *Proceedings, 1990 SRC Technical Conference*, pp. 102-105, October 1990.

56. Y. Leblebici and S. M. Kang, "An Integrated Hot-Carrier Degradation Simulator for VLSI Reliability Analysis," *Proceedings, International Conference on Computer-Aided Design*, pp. 400-403, November 1990.

57. S. M. Kang, "Regular CMOS Structures for VLSI," *Proceedings, International Workshop on CMOS VLSI Design* (Lausanne, Switzerland), September 1990.

58. S. M. Kang, "High-Speed CMOS Circuits," *Proceedings, International Workshop on CMOS VLSI Design* (Lausanne, Switzerland), September 1990.

59. Y. Leblebici, P. C. Li, S. M. Kang, and I. N. Hajj, "Hierarchical Simulation of Hot-Carrier Induced Damages in VLSI Circuits," *Custom Integrated Circuits Conference*, pp., 29.31-29.34, May 1991.

60. Y. H. Shih and S. M. Kang, "A New MOS Circuit Primitive for Fast Timing Simulation," *1991 International Symposium on Circuits and Systems*, pp. 2391-2394, May 1991.

61. Y. H. Shih and S. M. Kang, "ILLIADS: A New Fast MOS Timing Simulator Using Direct Equation-Solving Approach," *Proc. of 28th Design Automation Conference,* pp. 20-25, June 1991.

61. J. J. Morikuni, D. S. Gao, S. M. Kang, J. A. Priest, and C. L. Balestra, "New Circuit Models of Optical Logic Gates for Computer Simulation," *1991 Topical Meeting on Integrated Photonics Research*, pp. 67-68, April 1991.

62. S. M. Kang, "Simulation of Optoelectronic Integrated Circuits," *World Congress of Engineers and Scientists*, Seoul, Korea, Aug 1990.

63. J. M. Lee and S. M. Kang, "Testable CMOS Circuits for Logical Testability of Stuck-Open/Stuck-On Faults," *Midwest Symp. on Circuits and Systems*, May 1991.

64. P. Duchene, M. Declercq, and S. M. Kang, "An Integrated Layout System for Sea-of-Gates Module Generation," *Proceedings of the European Design Automation Conference*, pp. 237-241, February 1991.

65. M. Sriram and S. M. Kang, "A Parallel Min-Cut Technique for Standard Cell Placement Using a Modified Hopfield Neural Network," *Proc. of International Conference on Circuits and Systems*, pp. 894-897, Shenzhen, China, June 1991.

66. S. M. Kang, "Computer-Aided Design for VLSI (Invited Paper)," *Proc. of International Conference on Circuits and Systems*, pp. 1-5, Shenzhen, China, June 1991.

67. S. M. Kang, "Regular CMOS Structures for VLSI," *Proceedings, International Workshop on CMOS VLSI Design* (Lausanne, Switzerland), August 1991.

68. S. M. Kang, "High-Speed CMOS Circuits," *Proceedings, International Workshop on CMOS VLSI Design* (Lausanne, Switzerland), August 1991.

69. Y.-H. Shih, Y. Leblebici, and S. M. Kang, "New Simulation Methods for MOS VLSI Timing and Reliability," *Proc. of International Conference on Computer-Aided Design*, pp. 162-165, November 1991.

70. S. M. Kang, "Microelectronic and Optoelectronic Integration for Reliable High-Performance Systems," *Proc. KSEA/KOSEF Symposium*, January 1992.

71. J. Morikuni and S. M. Kang, "An Analysis of High-Frequency Amplifier Inductive Peaking," *1992 International Symposium on Circuits and Systems*, pp. 2848-2851, May 1992.

72. Sun, Y. Leblebici, and S. M. Kang, "Design-for-Reliability Rules for Hot-Carrier Resistant CMOS VLSI Circuits," *1992 International Symposium on Circuits and Systems*, pp. 1254-1257, May 1992.

73. Y. Leblebici and S. M. Kang, "One-Dimensional Transient Device Simulation Using a Direct Method Circuit Simulator," *1992 International Symposium on Circuits and Systems*, pp. 895-898, May 1992.

74. J. Morikuni, A. A. Ketterson, M. Tong, J.-W. Seo, K. Nummila, S. M. Kang, I. Adesida, and K. Y. Cheng, "A High Speed Integrated Optoelectronic Photoreceiver," *1992 International Symposium on Circuits and Systems*, pp. 1368-1371, May 1992.

75. A. Dharchoudhury and S. M. Kang, "Systematic Indentification of Correlated Device Parameters for Worst-Case Circuit Performance Analysis," *1992 VLSI Design,* Banglore, India, January 1992.

76. A. Dharchoudhury and S. M. Kang, "An Integrated Approach to Realistic Worst-Case Design Optimization of MOS Analog Circuits," *1992 Design Automation Conference*, pp. 704-709, June 1992.

77. W. Sun, Y. Leblebici, and S. M. Kang, "A Parametric Macro-Model Approach for Hot-Carrier Resistant CMOS VLSI Design," *1992 Custom Integrated Circuits Conference*, pp. 18.3.1-18.3.4, May 1992.

78. S. Kang, "Facing Nonlinearities Squarely for MOS VLSI Analysis (Invited Paper)," *A. Popov Society International Seminar on Nonlinear Circuits and Systems,* June 1992.

79. M. Sriram and S. M. Kang, "Detailed Layer Assignment for MCM Routing," *1992 International Conference on Computer-Aided Design,* pp. 386-389, November 1992.

80. Y. Leblebici, M. S. Unlu, and S. M. Kang, "A Novel Method for Mixed Device/Circuit Simulation of Optoelectronic Integrated Circuits," *Proc. IEEE Asia-Pacific Conference on Circuits and Systems,* pp. 460-465, Sydney, Australia, December 1992.

81. D. Cho, S. Raje, M. Sarrafzadeh, M. Sriram, and S. M. Kang, , "Crosstalk-Minimum Layer Assignment," *ACM/SIGDA Physical Design Workshop,* Lake Arrowhead, CA, April 1993.

82. D. Cho, S. Raje, M. Sarrafzadeh, M. Sriram, and S. M. Kang, , "Crosstalk-Minimum Layer Assignment," *1993 Custom Integrated Circuits Conference,* San Diego, CA, pp., 29.7.1-29.7.4 May 1993.

83. C. H. Diaz, C. Duvvury, S. M. Kang, and L. Wagner, "Electrical Overstress (EOS) Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices," *1992 EOS/ESD Symposium,* vol. 4, pp. 88-94, Dallas, TX, September 1992.

84. S. Ho and S. M. Kang, "Optoelectronic Memory Array for Switching and Interconnection Networks," *LEOS'92 Conference on Proc.,* pp. 592-593, Boston, MA, November 1992.

85. M. Sriram, S. M. Kang, "Performance-Driven MCM Routing Using a Second-Order RLC Tree Delay Model," *IEEE International Conference on Wafer Scale Integration,* pp. 262-267, January 1993.

86. J. Morikuni, M. Tong, K. Nummila, J. Seo, A. Ketterson, S. M. Kang, and I. Adesida, "A Monolithic Integrated Optoelectronic Receiver Using an MSM Detector," *1993 IEEE International Solid-State Circuits Conference*, pp. 178-179, San Francisco, CA, February 1993.

87. S. Sapatnekar, P. M. Vaidya, and S. M. Kang, "Feasible Region Approximation Using Convex Polytypes," *1993 IEEE International Symposium on Circuits and Systems*, pp. 1786-1789, Chicago, IL, May 1993.

88. E. J. Brauer and S. M. Kang, "Functional Verification of ECL Circuits Including Voltage Regulators," *1993 IEEE International Symposium on Circuits and Systems*, pp. 1710-1713, Chicago, IL, May 1993.

89. D. H. Cho and S. M. Kang, "An Accurate AC Characteristic Table Look-up Model for VLSI Analog Circuit Simulation Applications," *1993 IEEE International Symposium on Circuits and Systems*, pp. 1531-1534, May 1993.

90. M. Sriram and S. M. Kang, "Fast Approximation of the Transient Response of Lossy Transmission Line Trees," *1993 IEEE/ACM Design Automation Conference,* pp. 691-696, Dallas, TX, June 1993.

91. S. Sapatnekar, P. M. Vaidya and S. M. Kang, "Convexity-Based Algorithms for Design Centering," *1993 ICCAD*, Santa Clara, CA, pp. 206-209, Nov. 1993.

92. W. Jansz, W. Sun, Y. Leblebici, and S. M. Kang, "Fast Hot-Carrier Reliability Diagnosis Using Macro-models," *Proc. International Symposium on VLSI Technology Systems & Applications*, pp. 128-132, Taiwan, May 12-14, 1993.

93. B. Whitlock, E. Conforti, and S. M. Kang, "iFROST: Illinois fiber-optic and Optoelectronic Systems Took Kit for Simulation of Optical Interconnect Systems," *OFC '93*, San Jose, CA, May 1993.

94. J. Lockwood, C. Cheong, S. Ho, B. Cox, S. M. Kang, S. G. Bishop, and R. Campbell, "iPOINT Testbed for optoelectronic ATM Networking," *CLEO'93*, pp. 370-371, Baltimore, MD, February 1993.

95. M. Sriram and S. M. Kang, "iPROMIS: An Interactive Performance-Driven Multilayer M&M Router," *1993 IEEE Multichip Module Conference,* Santa Cruz, CA, pp. 170-173, March 1993.

96. C. Diaz, S. M. Kang, and C. Duvvury, "Thermal Failure Simulation for Electrical Overstress in Semiconductor Devices," *Proc. International Symposium on Circuits and Systems,* pp. 1389-1392, Chicago, IL, May 1993.

97. C. H. Diaz, C. Duvvury and S. M. Kang, "Studies of EOS Susceptibility in 0.6 μm nMOS ESD I/O Protection Structures," *15th EOS/ESD Symposium*, pp. 83-91, Orlando, FL, September 1993.

98. C. H. Diaz and S. M. Kang, "Circuit-Level Electrothermal Simulation for EOS/ESD Analysis," *SRC Techcon '93*, pp. 271-273, September 1993.

99. S. M. Kang and M. Sriram, "Multichip Modules for VLSI Systems Integration (Invited Paper), *International Conference on VLSI and CAD*, pp. 1/1-1.6, November 1993.

100. S. H. Ho, E. Conforti, and S. M. Kang, "Monolithic Optical Equalizer Array for Wavelength-Reusable and Topology-Reconfigurable WDM Local Area Networks," *1993 IEEE/LEOS Annual Meeting*, pp. 416-417, November 1993.

101. C. H. Diaz, C. Duvvury, and S. M. Kang, "Electrothermal Simulation of Electrical Overstress in Advanced nMOS ESD Protection Devices," *1993 IEEE Electron Devices Meeting*, pp. 131-134, December 1993.

102. E. C. Chang and S. M. Kang, "Transient Simulation of Lossy Transmission Lines Using Piecewise Recursive Convolution," *1993 International Symposium on Nonlinear Theory and Its Applications,* Waikiki, HI, December 5-9, pp. 329-334, 1993.

103. S. M. Kang, B. K. Whitlock, J. J. Morikuni, and E. Conforti, "Simulation of Optical Interconnects in High-Performance Computing and Communications," *1994 SPIE Meeting,* Los Angeles, CA, January 1994.

104. J. Kim, S. M. Kang, and S. S. Sapatnekar, "High Performance CMOS Macromodule Layout Synthesis," *1994 International Symposium on Circuits and Systems,* London, England, May 1994.

105. E. P. Olson and S. M. Kang, "State Assignment for Low-Power FSM using Genetic Local Search," *1994 International Symposium on Circuits and Systems,* London, England, May 1994.

106. J. Kim and S. M. Kang, "A New Triple-Layer OTC Channel Router," *1994 IEEE Custom Integrated Circuits Conference,* San Diego CA, pp. 647-650, May 1994.

107. D.-H. Cho and S. M. Kang, "A New Deep Submicron Compact Physical Model for Analog Circuits," *1994 IEEE Custom Integrated Circuits Conference,* San Diego, CA, pp. 41-44, May 1994.

108. C. C. Teng, W. Sun, and S. M. Kang, "iRULE: Fast Hot-Carrier Reliability Diagnosis using Marco-Models," *1994 IEEE Custom Integrated Circuits Conference,* San Diego, CA, pp. 421-424, May 1994.

109. E. Olson and S. M. Kang, "State Assignment for Low-Power FSM Synthesis using Genetic Local Search," *1994 IEEE Custom Integrated Circuits Conference,* San Diego, CA, pp. 140-143, May 1994.

110. T. Karnik and S. M. Kang, "A Hierarchical Partitioning of VHDL Structures," *1994 IEEE VHDL International User's Forum,* Oakland, CA, pp. 36-45, May 1994.

111. J. J. Morikuni and S. M. Kang, "Optoelectronic Simulation at the Device and Circuit Level," *IEEE LEOS Meeting,* Lake Tahoe, NV, pp. 8-9, July 1994.

112. T. Karnik, S. Ramswamy, S. M. Kang, and P. Banerjee, "Application of Algorithm Based Fault Tolerance to High-Level Synthesis of Signal Flow Graphs," *SPIE International Symposium on Optics, Imaging and Instrumentation,* pp. 760-776, San Diego, CA, July 1994..

113. T. Karnik, D. G. Saab, and S. M. Kang, "Hierarchical Mixed-Level Simulation of VHDL Descriptions," *1994 ASIC Conference,* Rochester, NY, pp. 170-173, September 1994.

114. H. Duan, J. W. Lockwood, and S. M. Kang, "FPGA Prototype Queueing Module for High Performance ATM Switching," *1994 ASIC Conference*, Rochester, NY, pp. 429-432, September 1994.

115. B. K. Whitlock, J. J. Morikuni, and S. M. Kang, "Optimizing Component Specifications in Optical Interconnects using Mixed-Level Simulation," *IEEE LEOS Annual Meeting,* Boston, MA, pp. 43-44, October 1994.

116. S. Ramaswamy, E. Rosenbaum, and S. M. Kang, "Circuit-Level Electrothermal Simulation Techniques for Designing Output Protection Devices," IEEE *Integrated Reliability Workshop,* Lake Tahoe, NV, pp. 79-82, October 1994.

117. A. M. Hill and S. M. Kang, "Genetic Algorithms Based Design Optimization of VLSI Circuits," *1994 International Conference on Evolutionary Computing,* Jerusalem, Israel, October 1994.

118. A. Dharchoudhury, S. M. Kang, K. H. Kim, and S. H. Lee, "Fast and Accurate Timing Simulation with Regionwise Quadratic Models of MOS I-V Characteristics," *1994 International Conference on Computer-Aided Design,* San Jose, CA, pp. 190-193, November 1994.

119. A. Dharchoudhury, S. M. Kang, H. Cha, and J. H Patel, "Fast Timing Simulation of Transient Faults in Digital Circuits," *1994 International Conference on Computer-Aided Design,* San Jose, CA, pp. 719-722, November 1994.

120. S. M. Kang, J. W. Lockwood, and H. Duan, "A Scalable Optoelectronic Network for Workstations," in *Defining the Global Information Infrastructure,* vol. CR56, S. F. Lundstrom, Ed. SPIE Press, 1994.

121. E. C. Chang and S. M. Kang, "Efficient Modeling and Simulation of Coupled Transmission Lines," *1995 IEEE Multichip Module Conference,* Santa Cruz, CA, pp. 152-157, January 1995.

122. W. Sun, E. Rosenbaum, and S. M. Kang, "Fast Timing Simulation for Submicron Hot-Carrier Degradation," *International Reliability Physics Symposium,* Las Vegas, NV, pp. 65-71, April 1995.

123. P. V. Mena, R. M. Lammert, S. M. Kang, and J. J. Coleman, "Demonstration of a Free-Space Optical Interconnect in a CMOS Chip," *Optoelectronic Interconnects II, SPIE Proc*., vol. 2400, no. 16, pp. 115-125, San Jose, CA, February 1995.

124. S. Ramaswamy, C. Duvvury, and S. M. Kang, "EOS/ESD Reliability of Deep Submicron nMOS Protection Devices," *International Reliability Physics Symposium,* Las Vegas, NV, pp., 284-291, April 1995.

125. A. M. Hill and S. M. Kang, "Determining Accuracy Bounds for Simulation-Based Switching Activity Estimation," *1995 Int. Symp. on Low-Power Des. (ISLPD)*, Dana Point, CA, pp. 215-220, April 1995.

126. Y.-K. Cheng and S. M. Kang, "Chip-Level Thermal Simulator to Predict VLSI Chip Temperature," *1995 IEEE Int. Symp. on Circuits and Syst*., Seattle, WA, pp. 1392-1395, May 1995.

127. J. W. Kim and S. M. Kang, "An Efficient Contact Placement for Custom Cell Layout Synthesis," *1995 IEEE Custom Integrated Circuits Conf*., Santa Clara, CA, pp. 275-278, May 1995.

128. T. Karnik, C. C. Teng, and S. M. Kang, "High-Level Hot Carrier Reliability-Driven Synthesis using Macromodels," *1995 IEEE Custom Integrated Circuits Conf*., Santa Clara, CA, pp. 65-68, May 1995.

129. A. M. Hill and S. M. Kang, "Accuracy Bounds in Switching Activity Estimation," *1995 Custom Integrated Circuits Conf*., Santa Clara, CA, pp. 73-76, May 1995.

130. E. J. Brauer and S. M. Kang, "An Analytical Method to Calculate Emitter Follower Delay using Trial Functions in Coupled Node Equations," *1995 IEEE Int. Symp. on Circuits and Syst*., Seattle, WA, pp. 1580-1583, May 1995.

131. M. Cynn and S. M. Kang, "Incremental Node Extraction Algorithms for Incremental Layout System," *1995 IEEE Int. Symp. on Circuits and Syst*., Seattle, WA, pp. 1691-1694, May 1995.

132. E. Conforti, B. K. Whitlock, J. J. Morikuni, and S. M. Kang, "Issues in the Modeling of Fiber Optic Systems," *Proc. 1995 SBMO/IEEE MTT-S Int. Microwave and Optoelectronics Conf.*, Vol. 1, Rio de Janeiro, Brazil, pp. 175-182, July 25, 1995.

133. B. K. Whitlock, E. Conforti, and S. M. Kang, "High-Level Software for Simulation of Fiber Optic Links," *Proc. Brazilian 13th Telecommun. Soc. Conf.*, Vol. 1, Aguas de Lindoia, Brazil, pp. 103-108, September 4, 1995.

134. S. Ramaswamy, P. Raha, E. Rosenbaum, and S. M. Kang, "EOS/ESD Protection Circuit Design for Deep Submicron SOI Technology," *1995 EOS/ESD Symp.*, Phoenix, AZ, pp. 212-217, September 1995.

135. H. Duan, J. W. Lockwood, and S. M. Kang, "An Efficient Input Queuing and Cell Scheduling Scheme for Scalable Ultra Broadband Optoelectronic ATM Switching," *SPIE Photonics East '95 Proc.*, Vol. 2608, Philadelphia, PA, pp. 197-208, October 24-26, 1995.

136. S. Ho and S. M. Kang, "Selective Switching - An Enabling Technology for High-Performance ATM Switch Fabric," *SPIE Photonics East '95 Proc.*, Vol. 2608, Philadelphia, PA, pp. 178-189, October 24-26, 1995.

137. A. Hossain and S. M. Kang, "Fuzzy Logic Based Cell Scheduling for Input-Buffered ATM Switches," *SPIE Photonics East '95 Proc.*, Vol. 2608, Philadelphia, PA, pp. 117-121, October 24-26, 1995.

138. P. K. Pepeljugoski, B. K. Whitlock, D. M. Kuchta, J. D. Crow, and S. M. Kang, "Modeling and Simulation of the OETC Optical Bus," in *IEEE LEOS '95 Conf. Proc.*, Vol. 1, San Francisco, CA, pp. 185-186, October 31, 1995.

139. T. Karnik and S. M. Kang, "An Empirical Model for Accurate Estimation of Routing Delay in FPGAs," *1995 IEEE Int. Conf. on Comput.-Aided Des.*, San Jose, CA, pp. 328-331, November 1995.

140. J. W. Kim and S. M. Kang, "A Timing-Driven Datapath Synthesis with Integer Programming," *1995 IEEE Int. Conf. on Comput.-Aided Des.*, San Jose, CA, pp. 716-719, November 1995.

141. K. Nahrstedt, A. Hossain and S. M. Kang, "A Probe-based Algorithm for QoS Specification and Adaptation," *Fourth International IFIP Workshop on Quality of Service,* Paris, France, March 6-8, 1996.

142. Y. K. Cheng, E. Rosenbaum and S. M. Kang, "A New Electrothermal Simulator for CMOS VLSI Circuits," *European Design & Test Conference*, Paris, France, pp. 566-570, March 6-8, 1996.

143. J. Lockwood, S. M. Kang, S. G. Bishop, H. Duan, and A. Hossain, "Development of the iPOINT Testbed for Optoelectronic Asynchronous Transfer Mode Networking," *International Conference on Information Infrastructure (Information Superhighway)*, Beijing, China, April 25-28, 1996.

144. C. C. Teng, Y. K. Cheng, E. Rosenbaum and S. M. Kang, "iTEM: A Chip-Level Electromigration Reliability Diagnosis Tool Using Electrothermal Timing Simulation," *IEEE Int. Reliability Physics Symposium,* pp. 172-179, April 21, 1996.

145. S. Ramaswamy, E. Li, E. Rosenbaum, and S. M. Kang, "Circuit-Level CDM-ESD and EOS Simulation of Submicron MOS Devices," *ESD/EOS Symposium,* pp. 316-321, Orlando, FL, September 10, 1996.

146. A. M. Hill, C. C. Teng, and S. M. Kang, "Statistical Results for Simulation-Based Maximum Power Estimation," *IEEE International Symposium on Circuits and Systems,* , vol. 4, pp. 13-16, Atlanta, GA., May 12-15, 1996.

147. H. Kutuk and S. M. Kang, "A Field Programmable Analog Array (FPAA) Using Switched Capacitor Techniques," *IEEE International Symposium on Circuits and Systems,* pp. 410-414, Atlanta, GA, May 12-15, 1996.

148. L. P. Yuan, C. C. Teng, and S. M. Kang, "Nonparametric Estimation of Average Power Dissipation in CMOS VLSI Circuits," *IEEE Custom Integrated Circuits Conference,* , pp. 225-228, San Diego, CA., May 5-8, 1996

149. Y. K. Cheng, C. C. Teng, A. Dharchoudhury, E. Rosenbaum and S. M. Kang, "A Chip-Level Electrothermal Simulator for Temperature Profile Estimation of CMOS VLSI Chips," *1996 IEEE International Symposium on Circuits and Systems,* pp. 580-583, vol. 4, Atlanta, GA., May 1996.

150. Y. K. Cheng, C. C. Teng, A. Dharchoudhury, E. Rosenbaum, and S. M. Kang, "iCET: A Complete Chip-Level Electrothermal Reliability Diagnosis Tool for CMOS VLSI Chips," *ACM/IEEE Design Automation Conference,* pp. 548-551, Las Vegas, NV., June 3-7, 1996.

151. C. C. Teng, Y. K. Cheng, E. Rosenbaum and S. M. Kang, "Hierarchical Electromigration Reliability Diagnosis for VLSI Interconnects," *ACM/IEEE Design Automation Conference,* pp. 752-759, Las Vegas, NV., June 3-7, 1996.

152. L. P. Yuan, C. C. Teng, and S. M. Kang, "Statistical Estimation of Average Power Dissipation in CMOS VLSI Circuits using Nonparametric Techniques," *ACM/IEEE Int. Symp. on Low Power Electronics and Des.,* Monterey, CA, , pp. 73-78, August, 1996.

153. S. Ramaswamy, E. Li, E. Rosenbaum, and S. M. Kang, "Circuit-Level CDM-ESD and EOS Simulation of Submicron MOS Devices," *1996 ESD/EOS Symp.,* Orlando, FL, pp. 316-321, September 10-12, 1996.

154. T. Li, S. Ramaswamy, and S. M. Kang, "EOS/ESD Protection Circuit Layout Extraction and Simulation," *SRC Techcon 96,* Phoenix, AZ, September 12-14, 1996.

155. T. Li, D. Suh, S. Ramaswamy, P. Bendix, E. Rosenbaum, A. Kapoor, and S. M. Kang, "Study of a CMOS I/O Protection Circuit Using Circuit-Level Simulation," *1997 Int. Rel. Phys. Symp.,* Denver, CO, April 7-10, 1997.

156. H. Duan, J. W. Lockwood, S. M. Kang, and J. D. Will, "A High-Performance OC-12/OC-48 Queue Design Prototype for Input-Buffered ATM Switches," pp. 20-28, Kobe, Japan, April 9-11, 1997.

157. T. Li, S. Ramaswamy, E. Rosenbaum, and S. M. Kang, "Circuit-Level Simulation and Layout Optimization for Deep Submicron EOS/ESD Output Protection Device," *IEEE Custom Integrated Circuits, Symp.,* pp. 159-162, Santa Clara, CA, May 5-8, 1997.

158. S. Y. Park, B. Vaduvur, and S. M. Kang, "Data Link Level Support for Handoff in ATM Network," *1997 Int. Conf. on Commun.,* Montreal, Canada, June 8-12, 1997.

159. J. W. Stroming, Y. Kang, T. S. Huang, and S. M. Kang, "New Architectures for Modified MMR Shape Coding," *1997 IEEE Int. Symp. on Circuits and Syst.,* pp. 1205-1208, Hong Kong, June 9-12, 1997.

160. S. M. Kang, H. Duan, J. W. Lockwood, and J. D. Will, "iiQueue, and QoS-Oriented Queue Module for Input-buffered ATM Switches," *1997 IEEE Int. Symp. on Circuits and Syst.*, pp. 2144-2147, Hong Kong, June 9-12, 1997.

161. L. P. Yuan, C. C. Teng, and S. M. Kang, "Statistical Estimation of Average Power Dissipation in Sequential Circuits," *ACM/IEEE Des. Automat. Conf.,* Anaheim, CA, June 9-13, 1997.

162. J. W. Kim and S. M. Kang, "An Efficient Transistor Folding Algorithm for Row-Based CMOS Layout Design," *ACM/IEEE Des. Automat. Conf.*, Anaheim, CA, June 9-13, 1997.

163. M. G. Lee, Y. J. Huh, M. C. Jung, T. Li, J. S. Lee, D. H. Song, Y. J. Lee, J. M. Hwang, and S. M. Kang, "Circuit-Level Simulation for Failure Analysis of Advanced CMOS ESD Protection Structures," *IEEE International Conference on VLSI and CAD*, Seoul, Korea, October 1997.

164. T. Li, Y. J. Huh, and S. M. Kang, "Automated extraction of parasitic BJTs for CMOS I/O circuits under ESD stress," *IEEE Int. Integrated Rel. Wkshp.*, Lake Tahoe, NV, pp. 585-587, October 1997.

165. T. Li, C. H. Tsai, Y. J. Huh, E. Rosenbaum, and S. M. Kang, "A new algorithm for circuit-level electrothermal simulation under EOS/ESD stress," *IEEE Int. Integrated Rel. Wkshp.*, Lake Tahoe, NV, pp. 130-131, October 1997.

166. S. M. Yoo and S. M. Kang, "A Boot-Strapped nMOS Charge Recovery Logic," *IEEE Great Lakes Symp. on VLSI,* pp. 30-33, Lafayette, LA, Feb. 19-21, 1998.

167. Y. J. Huh, M. G. Lee, J. S Lee, H. C. Jung, T. Li, D. H. Song, Y. J. Lee, J. M. Hwang, Y . K. Sung, and S. M. Kang, "A Study of ESD-Induced Latent Damage in CMOS Integrated Circuits," accepted for the *36th IEEE International Reliability Physics Symposium*, pp. 279-283, Reno, NV, March 30-April 2, 1998.

168. L. P. Yuan and S.M. Kang, "A Sequential Procedure for Average Power Analysis of Sequential Circuits," *IEEE/ACM Int. Symp. on Low Power Electronics and Design,* pp. 231-234, August 1997, Monterey, CA.

169. W. C. Choi and S. M. Kang, "Control of Bandwidth and Delay in Rate-Based Traffic Queuing," *U.S.-Korea Sci. and Technol. Symp.*, Chicago, IL, April 23-25, 1998.

170. S. Y. Park and S. M. Kang, "An Event-Driven Behavioral ATM Network Simulator," *U.S.-Korea Sci. and Technol. Symp.*, Chicago, IL, April 23-25, 1998.

171. T. Li, P. Bendix, D. Suh, Y. J. Huh, E. Rosenbaum, A. Kapoor, and S. M. Kang, "Optimum Design for a Two-Stage CMOS I/O ESD Protection Circuit," *IEEE Int. Symp. on Circuits and Syst.,* Monterey, CA, pp. 113-116, May 1998.

172. T. Li, C. H. Tsai, E. Rosenbaum, and S. M. Kang, "Modeling, Extraction and Simulation of CMOS I/O Circuits under ESD Stress," *IEEE Int. Symp. on Circuits and Syst.*, Monterey, CA, pp. 389-392, May 1998.

173. T. Li and S. M. Kang, "Layout Extraction and Verification for CMOS I/O Circuits," *IEEE/ACM Des. Automat. Conf.*, San Francisco, CA, pp. 291-296, June 15-19, 1998.

174. Ching-Han Tsai, Elyse Rosenbaum, Sung-Mo Kang, "Modeling, Extraction and Simulation of CMOS I/O Circuits under ESD Stress," *IEEE Int. Symp. on Circuits and Syst. (ISCAS'98),* Monterey, CA, June 1998.

175. C. W. Kim, S. M. Yoo, C. Kim, and S. M. Kang, "NMOS Energy Recovery Logic," *Proc. of IEEE Great Lakes VLSI Symp.,* Ann Arbor, MI, pp. 310-313, Feb. 1999.

176. S. M. Yoo and S. M. Kang, "No-Race Charge-Recycling Differential Logic (NCDL)," *Proc. of IEEE Great Lakes Symposium on VLSI,* Ann Arbor, MI, pp. 202-205, Feb. 1999.

177. K. W. Kim, T. T. Hwang, S. M. Kang, and C. L. Liu, "Logic Transformation for Low Power Synthesis," *1999 Des. Automat. and Test in Europe (DATE) Conf.,* Munich, Germany, pp. 158-162, March 1999.

178. K-W. Kim, S-M. Yoo, H. H. Chao, S-M. Kang, and C. L. Liu, "Low Power Logic Synthesis for a Finite-State Input Transition Power Dissipation Model," *Proc. of Int. Symp. on Circuits and Syst. (ISCAS'99),* Orlando, FL, pp. 111-114, May 31-June 2, 1999.

179. J. H. Chen and S. M. Kang, "A Mixed Frequency-Time Approach for Quasi-Periodic Steady-State Simulation of Multi-Level Modeled Circuits," *IEEE International Symposium on Circuits and Systems,* pp. 194-197, Orlando, FL, May 31-June 2, 1999.

180. I. C. Goknar, H. Kutuk and S. M. Kang, "Moment Components Technique for Passive Reduced Order Models for RLCG Interconnects," *IEEE TAU Workshop 99,* pp. 185-192, Monterey, CA, March 8-9, 1999.

181. J. H. Chen, K. M. Coperich, S. M. Kang and J. Schutt-Aine, "Parameter Extraction for a Microwave Micromachined Switch," *2nd Int. Conf. On Modeling and Simulation of Microsystems,* San Juan, Puerto Rico, pp. 190-193, April 19-21, 1999.

182. C. H. Tsai and S. M. Kang, "Standard Cell Placement for Even On-Chip Thermal Distribution," *IEEE International Symposium on Physical Design,* Monterey, CA, April 12-14, 1999.

183. D. Chen, E. Li, E. Rosenbaum and S. M. Kang, "Interconnect Thermal Modeling for Determining Design Limits on Current Density," *IEEE International Symposium on Physical Design,* Monterey, CA, pp. 172-178, April 12-14, 1999.

184. S. M. Yoo and S. M. Kang, "CMOS Pass-Gate Charge Recovery Logic (CPCRL)," *1999 IEEE Int. Symp. on Circuits and Syst. (ISCAS'99),* Orlando, FL, pp. 226-229, May 31, June 2, 1999.

185. T. Li, C. H. Tsai, E. Rosenbaum, and S. M. Kang, "Substrate Resistance Modeling and Circuit-Level Simulation of parasitic Device Coupling Effects for CMOS I/O Circuits under ESD Stress," *1999 IEEE/ACM Des. Automat. Conf.*, New Orleans, LA, pp. 549-554, June 21-25, 1999.

186. U. Ekambaram, S. M. Kang, and R. A. Saleh, "Behavioral Autonomous Steady-State Analysis using Broyden's Method," *Midwest Symp. on Circuits and Syst.*, Las Cruces, NM, August 1999.

187. E. Conforti, C. M. Gallep, A. C. Bordonalli, J. P. B. Custodio, S. Ho, and S. M. Kang, "Extinction Ratio Improvement using Feedforward Control of Semiconductor Optical Amplifier Gain," *1999 IEEE MTT-S, AP-5, and LEOS Int. Microwave and Optoelectron. Conf.*, Rio de Janeiro, Brazil, August 9-12, 1999.

188. E. Conforti, C. M. Gallep, A. C. Bordonalli, J. P. B. Custodio, S. Ho, and S. M. Kang, "Optical Carrier Reuse with Gain Compression and Feedforward Semiconductor Optical Amplifiers," *1999 IEEE MTT-S, AP-5, and LEOS Int. Microwave and Optoelectron. Conf.,* Rio de Janeiro, Brazil, August 9-12, 1999.

189. I. C. Goknar, H. Kutuk, and S. M. Kang, "Passive Model Order Reduction for RLCG Interconnects Via the Moment Matching Method," *European Conf. on Circuit Theory and Des. (ECCTD),* Rome, Italy, August 29-September 2, 1999.

190. Y. K. Cheng and S. M. Kang, "An Efficient Method for Hot-Spot Identification in ULSI Circuits," *IEEE Int. Conf. on Comput.-Aided Des.*, San Jose, CA, pp. 124-127, November 7-11, 1999.

191. K. W. Kim, S. M. Kang, and C. L. Liu, "Implication Graph Based Domino Logic Synthesis," *IEEE Int. Conf. on Comput.-Aided Des.*, San Jose, CA, November 7-11, 1999.

192. C. H. Tsai and S. M. Kang, "Efficient Transient Electrothermal Simulation by Reduced-Order Substrate Thermal Modeling," *IEEE Southwest Symp. on Mixed-Signal Des.*, San Diego, CA, February 27-29, 2000.

193. Q. Li and S. M. Kang, "Technology Independent Arbitrary Device Extractor," *IEEE Great Lakes VLSI Symp.,* Evanston, IL, March 2-4, 2000.

194. Q. Li and S. M. Kang, "Efficient Algorithms for Polygon to Trapezoid Decomposition and Trapezoid Corner Stitching," *IEEE Great Lakes VLSI Symp.*, Evanston, IL, March 2-4, 2000.

195. J. H. Chen and S. M. Kang, "Techniques for Coupled Circuit and Micromechanical Simulation," *Modeling and Simulation of Microsyst. Conf.*, San Diego, CA, March 27-29, 2000.

196. C. W. Kim, S. O. Jung, K. H. Baek, and S. M. Kang, "Parallel Dynamic Logic (PDL) and Speed-Enhanced Skewed Static (SSS) Logic," *IEEE Int. Symp. on Circuits and Syst.*, Geneva, Switzerland, May 28-31, 2000.

197. S.-M. Yoo and S.-M. Kang, "New High Performance Sub-1V Circuit Technique with Reduced Standby Current and Robust Data Holding," *IEEE Int. Symp. on Circuits and Syst.*, Geneva, Switzerland, May 28-31, 2000.

198. K. W. Kim, U. Narayanan, and S. M. Kang, "High-Performance Domino Logic Synthesis with Noise Constraints," *ACM/IEEE Design Automation Conf. (DAC),* Los Angeles, CA, June 5-9, 2000.

199. C. H. Tsai and S. M. Kang, "Fast Temperature Calculation for Transient Electrothermal Simulation by Mixed Frequency/Time Domain Thermal Model Reduction," *ACM/IEEE Design Automation Conf. (DAC),* Los Angeles, CA, June 5-9, 2000.

200. K. W. Kim, S. O. Jung, U. Narayana, C. L. Liu, and S. M. Kang, "Noise-Aware Power Optimization for On-Chip Interconnect," *International Symp. On Low Power Electronics and Design*, Rappalo, Italy, July 26-27, 2000.

201. J. Chen and S. M. Kang, "Model-Order Reduction of Weakly Nonlinear Systems with Taylor Series Expansion and Arnoldi Approach," *IEEE 43rd Midwest Symp. On Circuits and Systems*, Lansing, MI, Aug. 8-11, 2000.

202. K. H. Baek, K. W. Kim and S. M. Kang, "A Low Energy Encoding Technique for Reduction of Coupling Effects in SoC Interconnects," *IEEE 43rd Midwest Symp. On Circuits and Syst*., Lansing, MI, Aug. 8-11, 2000.

203. J. Moorman, J. Lockwood and S. M. Kang, "Real-Time Prioritized Call Admission Control in a Base Station Scheduler," *ACM WOWMOM*, Boston, MA, pp. 28-37, August 2000.

204. C. W. Kim, J. S. Lee, K. H. Baek, E. Martina, and S. M. Kang, "High-Performance Low-Power Skewed Static Logic in Very Deep-Submicron (VDSM) Technology," *IEEE Int. Conf. On Comp. Des*., Austin, TX, pp. 59-64, Sept. 17-20, 2000.

205. C. W. Kim, J. S. Lee, K. H. Baek, and S. M. Kang, "Low-Power Skewed Static Logic with Topology-Dependent Dual Vt," *13th Annual IEEE Int. ASIC/SOC Conf*., Washington, DC, pp. 310-314, Sept. 13-25, 2000.

206. S. Joshi, P. Juliano, E. Rosenbaum, G. Kaatz, and S. M. Kang, "ESD Protection for BiCMOS Circuits," *Proc. of IEEE Bipolar/BiCMOS Circuits and Technol. Mtg*., Minneapolis, MN, pp. 218-221, Sept. 24-26, 2000.

207. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Chip-Level Simulation for CDM Failures in Multi-Power ICs," *EOS/ESD Symp.,* Anaheim, CA, September 26-28, 2000. (**Best Student Paper Award**)

208. K. W. Kim, K. H. Baek, N. Shanbhag, C. L. Liu, and S. M. Kang, "Coupling-Driven Signal Encoding Schemes for Low-Power Interface Design," *IEEE Int. Conf. On Comput.-Aided Design,* San Jose, CA, pp. 318-321, Nov. 5-9, 2000.

209. S. Bucheli, J. R. Moorman, J. W. Lockwood, and S. M. Kang, "Compensation Modeling for QoS Support on a Wireless Network," *Globecomm 2000*, San Francisco, CA, Nov. 2000.

210. J. Zhou, C. Liu, J. H. Chen, and S. M. Kang, "Development of a Wide Tuning Range MEMS Tunable Capacitor for Wireless Communication Systems," *IEEE Int. Electron Device Meeting*, 2000.

211. J. H. Chen and S. M. Kang, "Computer-Aided Design of Mixed-Technology VLSI Systems," *IEEE Asia-Pacific Conf. On Circuits and Systems,* Tianjin, China, Dec. 2000.

212. J. H. Chen, J. Zou, S. M. Kang, and C. Liu, "Electro-Mechanical and Microwave S-Parameter Properties Of a Wide-Tuning Range MEMS Tunable Capacitor," *IEEE Conf. On Modeling and Simulation of Microsystems,* Hilton Head Island, SC, Mar. 19-21, 2001.

213. S. O. Jung, K. W. Kim and S. M. Kang, "Transistor Sizing for Reliable Domino Logic Design in Dual Threshold Voltage Technologies," *ACM 11th Great Lakes Symp. On VLSI,* West Lafayette, IN, Mar. 22-23, 2001.

214. S. M. Yoo, S. O. Jung and S. M. Kang, "Two-Level LFSR Scheme with Asynchronous Test Pattern Transfer For Low Cost and High Efficiency Built-In-Self-Test," *ACM 11th Great Lakes Symp. On VLSI,* West Lafayette, IN, Mar. 22-23, 2001.

215. S. O. Jung, K. W. Kim and S. M. Kang, "Noise Constrained Power Optimization for Dual Vt Domino Logic," *IEEE Int. Symp. On Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

216. J. H. Chen and S. M. Kang, "Model-Order Reduction of Nonlinear MEMS Devices Through Arclength-Based Karhunen-Loeve Decomposition," *IEEE Int. Symp..on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

217. S. M. Yoo, C. W. Kim, S. O. Jung, K. H. Baek, and S. M. Kang, "New Current-Mode Sense Amplifies for High Density DRAM and PIM Architectures," *IEEE Int. Symp. On Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

218. S. M. Yoo, S. O. Jung and S. M. Kang, "Low Cost and High Efficiency BIST Scheme with 2-Level LFSR and ATPT," *IEEE Int. Symp. On Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

219. K. W. Kim and S. M. Kang, "A Low-Power Reduced Swing Single Clock Flip-Flop," *IEEE Int. Symp. on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

220. Q. Li, Y. J. Huh, J. W. Chen, P. Bendix, and S. M. Kang, "Full Chip ESD Design Rule Checking," *IEEE Int. Symp. On Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

221. Q. Li, Y. J. Huh, J. W. Chen, P. Bendix, and S. M. Kang, "ESD Design Rule Checker," *IEEE Int. Symp. on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

222. C. W. Kim, K. W. Kim and S. M. Kang, "Energy Efficient Skewed Static Logic Design with Dual Vt," *IEEE Int. Symp. on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

223. K. W. Kim, S. O. Jung and S. M. Kang, "Coupling-Aware Minimum Delay Optimization for Domino Logic Circuits," *IEEE Int. Symp. on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

224. Q. Li and S. M. Kang, "Efficient Algorithms for Polygon to Trapezoid-to- Simple Polygon Decomposition for Resistance Extraction," *IEEE Int. Symp. on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

225. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Design-for-ESD Reliability in High-Frequency I/O Interfaces in Deep-Submicron CMOS Technology," *IEEE Int. Symp. on Circuits and Systems,* Sydney, Australia, May 6-9, 2001.

226. C. W. Kim and S. M. Kang, "A Low-Swing Clock Double-Edge Triggered Flip-Flop," *IEEE Symp. on Circuits,* June 2001.

227. K. W. Kim, S. O. Jung, P. Saxena, C. L. Liu and S. M. Kang, "Coupling Delay Optimization by Temporal Decorrelation Using Dual Threshold Voltage Technique," *ACM/IEEE Design Automation Conf.,* Las Vegas, NV, June 2001.

228. S. M. Kang and S. M. Yoo, "Circuit Solutions for Overcoming Ultra-Deep Submicron CMOS Leakage Currents, Noises and Power Consumption," *Proc. of Int. Tech. Conf. On Circuits, Systems, Computers and Communications (ITC-CSCC)*, Tokushima, Japan, pp. 1-4, July 10-12, 2001. **(keynote talk)**

229. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Understanding and Addressing the Noise Induced by ESD in Multiple Power Supply Systems," *IEEE Int. Conf. on Computer Design,* Austin, TX, pp. 406-411, Sept. 24-26, 2001.

230. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Noise-Aware Design for ESD Reliability in Mixed-Signal Integrated Circuits," *IEEE Int. ASIC/SOC Conf.,* Arlington, VA, pp. 437-441, Sept. 2001.

231. J. H. Chen and S. M. Kang, "Dynamic Modeling of MEMS Mirror Devices," *IEEE Electron Devices Meeting (IEDM),* Washington, DC, pp. 41.5.1-41.5.4, Dec. 2001.

232. I. C. Hwang and S. M. Kang, "A Self-Regulating VCO with Supply Sensitivity <0.15%-delay/1%-Supply," *IEEE Int. Solid-State Circuits Conf. (ISSCC),* San Francisco, CA, pp. 140-141, Feb. 3-7, 2002.

233. C. W. Kim, I. C. Hwang and S. M. Kang, "Low-Power Small-Area +/- 7.28pS Jitter 1GHz DLL-Based Clock Generator," *IEEE Int. Solid-State Circuits Conf. (ISSCC),* San Francisco, CA, pp. 142-143, Feb. 3-7, 2002.

234. S. O. Jung, K. W. Kim and S. M. Kang, "Dual Threshold Voltage Domino Logic Synthesis with Noise and Power Constraints," *Design Automation and Test in Europe (DATE),* Paris France, March 4-7, 2002.

235. S. O. Jung and S. M. Kang, "Skew-Tolerant High Performance Domino Logic," *IEEE Int. Symp. on VLSI,* Pittsburgh, PA, pp. 41-46, April 2002.

236. J. H. Chen, Jun Zou, C. Liu, and S. M. Kang, "Development of a MEMS Vertical Planar Coil Inductor," Fifth International Conf. On Modeling and Simulation of Microsystems, San Juan, Puerto Rico, pp. 344-347, April 22-25, 2002.

237. K. H. Baek, Myung-Jun Choe, Celso Souza, and S. M. Kang, "A Low-Power High-Speed BiCMOS Current Switch with Enhanced Spectral Bandwidth," *IEEE Int. Symp. on Circuits and Systems,* Phoenix, AZ, pp. 53-56, May 26-29, 2002.

238. R. K. Grube, Q. Wang, and S. M. Kang, "Design Limitations in Deep Sub-0.18um CMOS SRAM Circuits for High Performance On-Chip Cache Applications," IEEE Great Lakes Symposium on VLSI, pp. 94-97, April 18-20, 2002,.

239. G. Yang, S. O. Jung, S. H. Kim, and S. M. Kang, "A Low-Power 2.1GHz 32-bit Carry Lookahead Adder Using Dual Path All-N-Logic," IEEE Midwest Symposium on Circuits and Systems, Tulsa, OK, August 4-7, 2002.

240. Y. S. Kim, S. H. Kim, K. H. Baek, S. K. Kim, and S. M. Kang, "Multiple Trigonometric Approximation of Sine-Amplitude for High Speed Direct Digital Frequency Synthesizers," VLSI Symposium, Bombay, India, Jan. 2003.

241. S. Wu and S. M. Kang, "Modeling and Time-Domain Simulation of VSEL Using VHDL-AMS," IEEE Southwest Symposium on Mixed-Signal Design, May 2003.

242. Q. Wang and S. M. Kang, "An Optimal Design of Leak-Proof SRAM Cell Using MCDM Method," SPIE International Symposium on Microelectronics for the New Millennium, Gran Canaria, Spain, vol. 5117, pp. 478-484, May 19-21, 2003.

243. K. H. Baek, M.-J. Choi, E. Merlo, and S. M. Kang, "1-GS/s, 12-bit SiGe BiCMOS D/A Converter for High Speed DDFS," International Symp. on Circuits and Systems, Bangkok, Thailand, May 25-28, 2003.

244. K. H. Baek, M.-J. Choi, E. Merlo, and S. M. Kang, " Addressing a High Speed D/A Converter Design for Mixed-Mode VLSI Systems," IEEE Southwest Symp. On VLSI, pp. 21-26, 2003.

245. K. H. Baek, M.-J. Choi, and S. M. Kang, "An Efficient Calibration Technique for Systematic Current Mismatch of D/A Converters," International Symp. On VLSI, pp. 80-84, 2003.

246. S. M. Kang (Invited Keynote Address paper), "Elements of Low Power Design for Integrated Systems," IEEE International Symp. On Power Electronics and Design (ISPLED), Seoul, Korea, Aug. 25-27, 2003.

247. S. M. Kang, G. Yang, Q. Wang, and Z. Wang (Invited paper), " Gate Leakage Tolerant Circuits in Deep Sub-100nm CMOS Technologies," SPIE Conf. on Microelectronics, MEMS, and Nanotechnology, Perth, Australia, Dec. 10-12, 2003.

248. G. Yang, S. O. Jung, K. H. Baek, S. H. Kim, and S. M. Kang, "1.85 GHz 32-bit Carry Lookahead Adder Using Dual Path All-N-Logic, IEEE International Symposium on Circuits and Systems,Vancouver, Canada, May 23, 2004.

249. G. Yang, Z. Wang, and S. M. Kang, "Low Power High Performance Techniques for High Fan-In Dynamic Gates," 5th International Symposium on Quality Electronic Design, pp. 421-424, Santa Clara, CA, March 2004.

250. G. Yang, Z. Wang, and S. M. Kang, "Leakage-Proof Domino Circuit for Deep Sub-100nm Technologies," pp. 222-227, Mumbai, India, January 2004.

251. S. Wu and S. M. Kang, "Modeling of Metal Semiconductor Metal Photodetector Using VHDL-AMS," IEEE Behavioral Modeling and Simulation Conf. San Jose, Oct. 21-22, 2004.

252. S. H. Shin, K. R. Lee and S. M. Kang, " 3.48mW 2.4GHz Range Frequency Synthesizer Architecture with with Two point Channel Control for Fast Settling Performance", IEEE International SOC Conf., pp. 3-6, Santa Clara, CA, September 2005.

253. G. Yang, Y. S. Kim and S. M. Kang, "Current Mode Multi-Level Simultaneous Bidirectional I/O Scheme For Chip-to-Chip Communications," IEEE International Symp. On Circuits and Systems, Kobe, Japan, May 23-25, 2005.

254. S. M. Kang, "The Future of IT Education and Research," Proc. of the Hokkaido Information University International Forum 2005, pp. 24-31 (English), pp. 32-39 (Japanese), Ebetsu, Hokkaido, Japan, Oct. 2005.

255. S. Shin, K. Lee and S. M. Kang, " Low-Power 2.4GHz CMOS Frequency Synthesizer With Differently Controlled MOS varactor," IEEE Interantional Symp. on Circuits and Systems, pp. 553-556, Kos, Greece, May 2006.

256. S. Shin, K. Lee, and S. M. Kang, "A 4-Gb/s/pin Current Mode 4-Level Simultaneous Bidirectional I/O with Current Mismatch Calibration," IEEE International Symp. on Circuits and Systems, pp. 1007-1010, Kos, Greece, May 2006.

257. Y. Kim, S. Shin, and S. M. Kang, "A High Speed Low Power Accumulator for Direct Digital Frequency Synthesizer," IEEE MTT-S International Symp., pp. 502-505, June 2006.

258. S. Shin, K. Lee, and S. M. Kang, "4.2mW CMOS Frequency Synthesizer for 2.5GHz ZigBee Application with Fast Settling Time Performance," IEEE MTT-S International Symp., pp. 411-414, June 2006.

259. J. H. Park, S. M. Kang, Y. Zhang, K. Fukutani, and A. Shakouri, "Three-Dimensional Electro-Thermal Modeling of Thin-Film Micro-Refrigerator for Site-Specific Cooling of VLSI ICs," IMAPS 39th International Symp. on Microelectronics, pp. 883-890, San Diego, CA, Oct. 8-12, 2006.

260. J. Hu, Y. Liu, A. Maslov, C. Z. Ning, R. Dutton, and S. M. Kang, " Simulation of P-N Junction Properties of Nanowires and Naowire Arrays," accepted for Photonics West 2007, San Jose, CA, Jan.25-27, 2007.

261. H. Schmidt, A. Shakouri, M. Isaacson, and S. M. Kang, "Roles of Bioelectronics for Quality of Life," (Invited Paper), Proc. of the 32nd European Solid-State Circuits Conf., pp. 33-41, Montreux, Switzerland, Sept. 2006.

262. Y. S. Kim and S. M. Kang, "Programmable High Speed Simultaneous I/O," International Symposium on Quality Electronic Design, pp. 416-419, San Jose, CA, March 2007.

263. A.B. Kahng, S. M. Kang, W. Li and B. Liu, "Analytical Thermal Placement for VLSI Improvement and Minimum Process Variation," International Conference on Computer Design, pp. 71-77, Oct. 2007.

264. J.H. Park, X. Wang, A. Shakouri, and S. M. Kang, "Fast Calculation of Temperature Profiles of IC Chips with High Spatial Resolution," Semiconductor Thermal Measurement, Modeling, and Management Symposium (Semi-Therm 24), pp. 51-55, San Jose, March 16-20, 2008.

265. J.H. Park, A. Shakouri, and S. M. Kang, "Fast Evaluation Transient Hot Spots in VLSI ICs in Packages," 9th International Symposium on Quality Electronic Design (ISQED '08), pp. 600-603, San Jose, March 17, 2008.

266. S. Shin, S. Yun, S. Cho, J. Kim, M. Kang, W. Oh and S. M. Kang, "0.18um CMOS Integrated Chipset for 5.8 GHZ Systems with +10dBm Output Power," IEEE ISCAS 2008, Seattle WA, May 18-21, 2008.

267. Y. S. Kim and S. M. Kang, "A 8-Gb/s/pin Current Mode Simultaneous Bidirectional I/O," IEEE ISCAS 2008, Seattle WA, May 18-21, 2008.

268. J. Jung, K.H. Baek, S. I. Lim, S. Kim, and S. M. Kang, "1.25 Gsamples/s DAC for a WPAN," IEEE ISCAS 2008, Seattle WA, May 18-21, 2008.

269. K. Maize, X. Wang, J.H Park, J. Christofferson, S. M. Kang, A. Shakouri, "High Speed Transient Thermal Characterization and Simulation of Integrated Circuits," 1st International Symposium on Thermal Design and Thermophysical Property for Electronics, Tsukuba, June 18-20, 2008. (Invited)

Bulletins

1. A. T. Yang and S. M. Kang, "iSMILE User's Manual," CCSM Report No. 88-62, UILU-ENG-88-0406.

2. J. J. Morikuni and S. M. Kang, "Computer Simulation of Optical Logic Gates," Report to McDonnell-Douglas 1990.

3. S. M. Kang and I. N. Hajj, "VLSI Design for Reliability-Hot Electron," Final Project Report to Rome Laboratory, March 1991.

4. C. Diaz and S. M. Kang, "Modeling and Simulation of EOS Failures in IC and Development of Design Guidelines," 4Q91, 1Q92, 2Q92, 3Q92, 4Q92, Report to Texas Instruments, January 1992- December 1992.

5. S. M. Kang, "Computer-Aided Design of Optoelectronic Subsystem," IEEE Report on Packaging, Interconnects, Optoelectronics for the Design of Parallel Computers Workshop, pp. 19-29, Schaumburg, IL, Mar. 1992.

6. M. Sriram and S. M. Kang, "A New Layer Assignment Approach for MCMs," Technical Report UIUC-BI-VLSI-92-01.

7. J. J. Morikuni and S. M. Kang, "An Analysis of Inductive Peaking in Photoreceiver Designs," Technical Report UIUC-BI-VLSI-92-02.

8. M. Sriram and S. M. Kang, "Efficient Approximation of Time Domain Response of Lossy Coupled Transmission Line Trees," Technical Report UIUC-BI-VLSI-91-03.

9. Izzet Cem Goknar, Haydar Kutuk, and Sung-Mo (Steve) Kang, "Moment Components: A New Tool for Obtaining Passive Reduced Order Models," CSL Technical Report, # UILU-ENG-98-2224 (DAC-68), October 1998.

10. Ki-Wook Kim, C. L. Liu, and Sung-Mo Kang, "Implication Graph Based Domino Logic Synthesis," CSL Technical Report, UILU-ENG-99-2206 (DAC-72), April 1999.

Magazine Articles and Licenses

1. Engineers Week Message by Silicon Valley Engineering Council President," San Jose Business Journal, Feb. 2003.

2. Engineering a Dream," Santa Cruz Sentinel Newspaper, July 21, 2002.

3. 'Foundation for Greatness: Head of UCSC's Engineering School Aims to Build a Top-Rated Program," Santa Cruz Sentinel Newspaper, July 22, 2002.

4. "Designing Hot-Carrier Resistant VLSI Circuits," Semiconductor International, Sept. 1991.

5. "The ILLIADS' ODYSSEY," Illinois Quarterly, Jan/Feb. 1991.

6. iSMILE Program, Licensed to University of Illinois.

7. ILLIADS Program, Highlighted in Illinois Quarterly, Semiconductor International.

8. iEDISON 3.0 Program, Licensed to University of Illinois.

9. iETSIM Program, Licensed to University of Illinois and Semiconductor Research Corp.

10. ILLIADS Program, Licensed to University of Illinois and then to Deutsch Research Incorp.

11. iFROST Program, Licensed to University of Illinois and then to RSoft Inc.

UNIVERSITY SERVICE

Circuits and Signal Processing Committee University of Illinois, 1985-1995 (Chair 1991)

University Senate, University of Illinois, 1986-87, 1992-1994

Graduate Committee, Dept. of ECE, University of Illinois, 1986-1989

Graduate Seminar Committee, Dept. of ECE, University of Illinois, 1986-1990, 1992-1994

Research Thrust Leader, NSF Engineering Research Center, University of Illinois, 1987-1996

Associate Director, NSF Engineering Research Center, University of Illinois, 1987-1995

Chairman, Ph.D. Qualifying Examination Committee, University of Illinois, 1988

Department Advisory Committee, University of Illinois, 1988-1989

CSL (Coordinated Science Laboratory) Policy and Planning Committee, University of Illinois, 1989-1990

ICAP (Illinois Computer Affiliates Program) Co-Chairman, University of Illinois, 1990

Chair, Circuits and Signal Processing Area, University of Illinois, 1991-1995

ICAP, Chairman, University of Illinois, 1991

Thrust Leader, Center for Optoelectronics Science and Technology (COST), 1993-1996

Department Head of Electrical and Computer Engineering, University of Illinois, 1995-2000

Campus Critical Research Initiative Proposal Review Board, University of Illinois, 1995

College Promotion and Tenure Committee, University of Illinois, 1995

Course Director of ECE 382 (Large-Scale Integrated Circuits), University of Illinois, 1985-2000

Course Director of ECE 482 (Physical VLSI Design), University of Illinois, 1986-2000

Chair, Faculty Search Committee, University of Illinois, 1995-2000

Member, Beckman Institute Steering Committee, University of Illinois, 1995-2000

Chair, Tykociner Lecture Committee, University of Illinois, 1996-2000

UC Santa Cruz Dean, Baskin School of Engineering, 2001-2007

UC Santa Cruz Board of Trustees (honorary member), 2001-2007

UC Santa Cruz Provost Advisory Council, 2001-2007

UC Santa Cruz Advisory Committee for Facilities, 2001-2007

UC Santa Cruz MBEST Oversight Committee, 2001-2006

UC Santa Cruz Academic Planning Council, 2001-2006

UC Santa Cruz Academic Instruction and Research Steering Committee, 2003-2007

UC Santa Cruz Communications Advisory Committee, 2002-2007

California Institute for Science and Innovation CITRIS Executive Committee, 2001-2007

California Institute for Science and Innovation QB3 Executive Committee, 2001-2003

UC Santa Cruz, Chancellor's Advisory Committee on Educational Partnership Program Chair, 2003-2007

OUTSIDE PROFESSIONAL ACTIVITIES

IEEE Standards Board Liaison Representative - 1977 to 1980

Editorial Board Member, International Journal of Circuit Theory and Applications-1984 to Present

Editor of Physical Design, IEEE Design and Test of Computers - May 1984 to July 1988

ADCOM Member, IEEE Circuits and Systems Society - January 1985 to December 1987

Associate Editor, IEEE Circuits and Devices Magazine - March 1987 to December 1989

Founding Chairman, Technical Comm. on VLSI Systems and Applications, IEEE Circuits and Systems Society - July 1987 to May 1989, May 1993 to December 1994

Secretary and Treasurer, IEEE Circuits and Systems Society - January 1988 to December 1988

Associate Editor, Circuits, Systems and Signal Processing Journal - January 1989-1992

Associate Editor, IEEE Transactions on Circuits and Systems - June 1989 to May 1991

Administrative Vice President, IEEE Circuits and Systems Society, 1989

President-Elect, IEEE Circuits and Systems Society, 1990

President, IEEE Circuits and Systems Society, 1991

IEEE Circuits and Systems Society Fellow Committee, 1991-2002

Member, Steering Committee, IEEE Multichip Module Conference, 1991-1995

NSF Review Panel, 1992-1995

Member, IEEE Technical Activities Board Administration Council, 1992

Chair, System Implementation Subcommittee, IEEE Multichip Module Conference, 1992-1994

Past President, IEEE Circuits and Systems Society, 1992

Member, IEEE TAB Administration Council, 1992

IEEE Circuits and Systems Society Nominations Committee Chair, 1993

IEEE Computer Society Fellow Committee, 1994

Chair, IEEE Transactions VLSI Systems Best Paper Award Technical Program Committee 1994-1997

Technical Program Chair, IEEE Asia Pacific Conference on Circuits and Systems 1994-1996

Technical Program Chair, IEEE International Symposium on Circuits and Systems 1994-1997

Member, IEEE LEOS Society Engineering Achievement Award Committee 1996

Program Co-Chair, IEEE Great Lakes VLSI Symposium Urbana, IL, 1997

Member Editorial Board, Proc. of the IEEE, 1996 - Present

Member, Steering Committee, International Symposium on Physical Design, 1996

Member, Technical Program Committee International Symposium on Physical Design, 1997

Secretary (President Elect), National EE Department Heads Assoc. (NEEDHA), 2000

ASEE Engineering Deans Council, 2001-2007

AAAS, 1996-present

Member, ASEE Policy Committee, 2003-2007

Chair, IEEE Transactions on VLSI Systems Best Paper Award Committee, 1994-1997

Member, IEEE CAS Meritorious Service Awards Committee 1994-1996

Member, IEEE CAS Education Award Committee 1994-1996

Member Steering Committee, IEEE Multichip Module Conference, 1991-1995

Member, International Steering Committee, IEEE Asia-Pacific Conference on Circuits & Systems, 1991-96

Editorial Board Member, Circuits Systems and Signal Processing, Birkhauser.

Program Committee, Southwest Symp. on Mixed-Signal Des., 1999

Chair, IEEE Circuits and Systems Society Technical Achievement Committee, 1999

Member, Technical Program Committee, IEEE International Symposium on Physical Design, 2002-2003

Member, Technical Program Committee, IEEE International Conf. On Microelectronic Systems Education, 2003

Member, Program Committee, SPIE Conf. on Microelectronics, MEMS, and Nanotechnology, 2003

Founding Member, IEEE-CAS Technical Committee on Nanoelectronics and Giga-Scale Systems, 2003

Member, International advisory committee for SOC Design Conference (SDC), 2003

General Chair, IEEE International Conference on System-On-a-Chip Conference (SOCC), September 2004

Chair, IEEE Circuits and Systems Society Technical Achievements Award Committee, 2004

External Advisory Board Member, Northwestern University, 1997-2000

External Advisory Board Member, Hong Kong University of Science and Technology, 1997-2005

External Review Board Member, Hong Kong Research Grants Council, present

External Review Board, Member, University of Alberta, Canada, 1999

Board Member, NEEDHA (National EE Heads Association) 1999-2000

Member, NSF Board of Visitors, 2000

Member, NSF Career Award Panel, 2002

President, Silicon Valley Engineering Council 2002-2003

State of California Leader for ASEE Engineering Deans Capitol Hill visit 2003, 2004

Member, NSF Review Panel for Science, Technology, Engineering, and Mathematics (STEM) Education, 2004

International Reviewer, National Science and Engineering Research Council of Canada, 2004

Co-General Chair, IEEE International Symposium on Circuits and Systems in 2012, Songdo, Korea, 2007-present

Member, Executive Board, Central Valley Higher Education Consortium, 2007-present

Member, International Review Board, Seoul National University, 2008-present

EDITORSHIP OF JOURNALS

Special Guest Editor, Proc. of the IEEE, On-Chip Thermal Engineering, Aug. 2006

Special Guest Editor, Proc. of the IEEE, Interconnections-Addressing the Next Challenge of IC Technology, Part 1, April 2001

Special Guest Editor, Proc. of the IEEE, Interconnections-Addressing the Next Challenge of IC Technology, Part 2, May 2001

Founding Editor-in-Chief, *IEEE Trans. on VLSI Systems,* 1992-1994

Special Guest Editor, *International Journal on Circuit Theory and Applications*, Nov. 1991 Issue

Special Guest Editor, *International Journal on Circuit Theory and Applications*, jointly with Professor P. DeWilde in The Netherlands, on Fundamental Methods for Computer-Aided Design for the October 1988 issue

Special Guest Editor, *IEEE Design and Test of Computers*, June 1987 issue on Physical Design of 32-bit Microprocessors

Editorial Board Member, *International Journal of Circuit Theory and Applications*, June 1984-present

Editor, Physical Design, *IEEE Design and Test of Computers*, 1984-1988

Editorial Board Member, Circuits, Systems and Signal Processing, 1986-2006

Editor of Digital Electronics, *IEEE Circuits and Devices Magazine*, 1987-1989

Associate Editor, *IEEE Transactions on Circuits and Systems*, June 1989 to May 1991

Associate Editor, *Circuits, Systems, and Signal Processing Journal*, Jan. 1989 to Dec. 1990

Editorial Board Member, Proc. of the IEEE, 1996-2005

International Advisory Board Member, IEICE Trans. On Fundamentals of Electronics, Communications and Computer Sciences, Engineering Sciences Society of Japan, 2000-present

Co-Series Editor, Advances in CAD for VLSI Book Series, Elsevier Science

Reviewer, *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, *IEEE Trans. on Electron Devices, IEEE Transactions on Circuits and Systems, IEEE Journal of Solid-State Circuits, International Journal of Circuit Theory and Applications*, Addison-Wesley Publishing Company, Prentice-Hall, Inc., McGraw-Hill, Springer-Verlag, Princeton Press, NSF

CONSULTING ACTIVITIES

ZMOS Technology Inc., Co-Founder and Chairman, 2002-present

Cadence/Celestry, Chairman, Technical Advisory Board, 2000-2005

Nanno Solutions, Technical Advisor 2006-2007

BTA Technology Inc., Board of Directors, 2000-2003

Rockwell Science Center, Technical Consultant, 2001-2002

Apache Design Automation, Technical Advisory Board, 2001-2004

Avanti Corp. July 1996-1999

Texas Instruments, 1998-1999

Samsung Electron Co., Dec. 1995 to May 1996

Anagram Inc., Board of Directors, Aug. 1993 to July 1996

Teltech, Inc., Aug. 1989-2000

Motorola, Inc. August 1990

MCC, Austin, TX, November 1988

AT&T Bell Laboratories, Allentown, PA, Murray Hill, Holmdel, NJ, Dec. 1988-1990

RESEARCH AREAS

Low Power Digital Integrated Circuits

Application Specific Integrated Circuits (ASICs)

Wafer-level VLSI Reliability

Computer-Aided Design of VLSI Circuits and Systems

Computer-Aided Design of OEICs

OEIC Systems and Optical Interconnects

Fully Optical Networks

Nanoelectronics

GRADUATE THESES COMPLETED UNDER DIRECT SUPERVISION (Since 1998):

(a) **M.S. Degrees Granted:** 40 (partial list)

J. Moorman	1998
M. Bossardt	1998 Swiss Federal Institute of Technology at Lausanne (**Best Thesis Award**)
S. Dixon	1998
D. Chen	1999
V. Nishar	1999
J. Katzenstein	2000
G. Yang	2003 UCSC
Q. Wang	2003 UCSC
A. Barangan	2003 UCSC

Z. Wang	2004 UCSC
P. Holm	2005 UCSC
W. Li	2005 UCSC

(b) **Ph.D. Degrees Granted (list of last 5 years)** 54

J. S. Lee	2001
C. W. Kim	2001
S. M. Yoo	2001
K. H. Baek	2002
S. O. Jung	2002
G. Yang	2004 UCSC
S. Wu	2005 UCSC
W. Li	2007 UCSC
Y.S. Kim	2008 UCSC
J. Hu	2008 UCSC

(c) **Ph.D. Thesis Students Supervised at UCSC:** 1

J. H. Park

POST DOCTORAL RESEARCHERS AND VISITORS HOSTED

J. M. Lee, 1991-1992, Korea, Kwandong University

D. Y. Han, 1992-1993, Korea, Kunkook University

Y. Leblebici, 1990-1993, Turkey, Technical University of Istanbul

E. Conforti, 1992-1994, Brazil, University of San Paolo

Y. Leblebici, 1994, 1997, Turkey, Technical University of Istanbul

C. Goknar, 1995-1998, Turkey, Technical University of Istanbul

M. K. Lee, 1996-1997, Yonsei University, Korea

Y. J. Huh, 1997-1998 LG Semicon, Korea

J. Lockwood, 1993-1999, UIUC

I. C. Hwang, 2000-2001, Korea University

H. B. Kim, 2000, Samsung Electron Company

S. W. Kim, 2001-2002, Korea University

S. Kim, 2001-2002, Korea University

J. H. Choi, 2001, Samsung Electron Company

D. Axelrad 2002, University of Grenoble, France

I.Shim, 2002, Korea University

Georg Kriebel, 2002-2003, Swiss Federal Institute of Technology at Lausanne

S. H. Shin, 2004-2006, Korea Advanced Institute of Science and Technology

S. I. Chae, 2005-2006, Seoul National University, Korea

Y. J. Song, 2005-2006, Konyang University, Korea

S. I. Lim, 2007-2008, Seokyung University, Korea

S. H. Shin, 2007- , KAIST

K. M. Kim, 2007- , KAIST

Y. S. Kim, 2008, UCSC

C. W. Kim, 2008-2009, Samsung Electronics, Korea

M. S. Son, 2008-2010, Sunchon University, Korea

J. J. Jung, 2007-2009, Korea University, Korea

P. Meinerzhagen, 2008, EPFL, Switzerland

OTHER SCHOLARLY ACTIVITIES

Distinguished Lecturer, University of Notre Dame, 1992

Distinguished Lecturer, University of Washington, 1991

Associate in The Center for Advanced Study, UIUC, 1991-1992

NSF Review Panel, Washington, DC, 1992

Distinguished Lecturer, Iowa State University, 1992

Invited Speaker, National Science Foundation Workshop, 1993

Invited Speaker, University of Washington, 1993

Distinguished Lecturer; National Research Council, Republic of China, 1993

Distinguished Lecturer, International Conference on VLSI and CAD, Korea 1993

Plenary Speaker, 1992 EOS/ESD Symposium, Dallas, TX, 1993

Invited Speaker, High Speed Interconnects Workshop, Santa Fe, NM, 1993

Invited Speaker, OSA Symposium, Toronto, Canada, 1993

Plenary Speaker, 1995 IEEE International Symposium on Circuits and Systems, 1995

Distinguished Lecturer, Asia-Pacific Conference on Circuits and Systems, 1994

Distinguished Lecturer, IEEE Circuits and Systems Society, 1994-1996

Invited Speaker, SPIE Photonics/East, 1994

Technical Program Chair, 1996 IEEE Asia-Pacific Conference on Circuits and Systems, Seoul, Korea, 1996

Technical Program Chair, 1997 IEEE International Symposium on Circuits and Systems, Hong Kong, 1997

Lecturer, Low Power Memory Design, Monterey, CA, April 1997

Lecturer, Low Power Memory Design, Lausanne, Switzerland, July 1997

Invited Talk, University of Karlsruhe, Germany, July 1997

Invited Talk, National University of Singapore, January 1998

Invited Talk, Korean Advanced Institute of Science and Technology, January 1998

Invited Talk, Technical University of Munich, Germany, July 1998

Invited Talk, Motorola Corp. Munich, Germany, Aug. 1998

Invited Talk, Tsinghua University, China, Dec. 2000

Invited Talk, Tokushima University, Japan, July 2001

Invited Talk, New York Chapter of KSEA, November 2001

Invited Talk, Plenary, "On-chip Thermal Engineering," Int. Symp. on Physical Design, San Diego, CA, Apr. 2001

Invited Talk, "UCSC School of Engineering," UC Board of Regents, Feb. 2002

Invited Talk, "Three Tenors of Technology for the 21st Century," Korean-American Chamber of Commerce of Silicon Valley, March 28, 2002

Invited Talk, "UCSC Engineering Programs," Cabrillo Kiwanis Club, Aptos, Oct. 2002

Invited Talk, UK House of Lords Science and Technology Committee, "Innovations in Microprocessors," June 10, 2002, Stanford University

Invited Talk, Santa Cruz Technology Symposium Keynote Address, February 23, 2002

Invited Talk, Korean Advanced Institute of Science and Technology (KAIST), June 2002

Invited Talk, "A Brief Highlight of Korean-American Engineers," at Centennial Celebration of Korean Immigration To United States Symposium, August 17, 2002, Falls Church, VA

Invited Talk, "UCSC Engineering Programs," Cabrillo College, Oct. 23, 2002

Invited Talk, " Industry-University Collaboration for Curriculum Development," Stanford University-KAIST Technology Forum, Stanford University, June 17, 2003

Invited Talk, "Building Engineering Programs for the 21st Century," IEEE Circuits and Systems Chapter Inauguration Meeting, San Jose, CA, June 16, 2003

Invited Talk, C. M. Lee Scholarship Award Ceremony, San Jose, CA, June 28, 2003

Invited Lectures, "Design for Manufacturability," KAIST, Taejon, Korea, Aug.12, 2003

Invited Talk, Santa Cruz Rotary Club, " Engineering for the 21st Century," June 3, 2004

Invited Talk, " Micro/Nanoelectronics for Life Systems," 2004 European Workshop for Microelectronics Education, Swiss Federal Institute of Technology, Lausanne, Switzerland, Apr.14-15, 2004

Invited Lecture, "Elements of Low Power Design," IEEE Circuits and Systems Society Distinguished Lecturer's Tour Lecture, Universidad Nacional del Sur, Bahia Blanca, Argentina, Nov. 19, 2004

Invited Talk, "Engineering Education for the 21st Century," IEEE Education Society-Silicon Valley Chapter, December 1, 2004

Invited Talk, "Education for Global Technological Leadership in the 21st Century," UKC 2005 Conference, UC Irvine, August 13, 2005

Invited Talk, "Future R&D Directions," UKC 2005 Conference, UC Irvine, August 12, 2005

Invited Lecture, "Design of Deep Submicron VLSI," ECCTD Conference, Cork, Ireland, September 2, 2005

Kenynote Talk, "Challenges and Innovations for Development of SOCs," International SOC Conference, Seoul, Korea, Oct. 21, 2005

Keynote Talk, "The Future of IT Education and Research," Hokkaido Information University International Forum," October 14, 2005

Keynote Talk, "Roles of Bioelectronics for Quality of Life," 32nd European Solid-State Circuits Conference, Montreux, Switzerland, Sept. 2006

Keynote Talk, "Nanobiotechnology for Quality of Life," IEEE Nanotechnology Symposium, Sunnyvale, CA, July 27, 2007

Keynote Talk, "Higher Education for the 21st Century," 2007 U.S.-Korea Conference, Washington D.C., August 11, 2007

Keynote Talk, "Global Leadership in Science and Technology," Global HR Forum, Seoul, Korea, Oct. 25, 2007

Keynote Talk, "To be VIP Scientists and Engineers," 2008 U.S.-Korea Conference, San Diego, CA, August 16, 2008

PROFESSIONAL IMPROVEMENT

Quality Control Workshop, 1990

University of Illinois Dean's Undergraduate Advising Workshop, 1993

National Institute of Teaching Effectiveness, June 1993

Dean's Workshop on Teaching: Tradition vs. Innovation, October 1993

Provost's New Administrators Orientation Workshop, September 1995

Provost's Pew Table Workshop, October 1995

Dean's Workshop on Partnership for Illinois, November 1995

NTU/Undergraduate Teaching Improvement, January 1996

Workshop on Investigation Techniques, Preparation of Findings and Mediation, January 1996

Sexual Harassment Workshop, University of Illinois, 1997

Budget Reform Workshop, University of Illinois, 1997

Presidential Retreat, University of Illinois, 1999

UC Management Institute, 2002

UCSC Chancellor's Retreat, 2001-2006

Sexual Harassment Training, University of California, 2008